NIELIT CALICUT

(Autonomous Scientific Society of Ministry of Electronics & Information Technology, Govt. of India)

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TENDER ENQUIRY **By Speed Post**

Ref. No.: 2(1146)/2019-20 /ASICEVKIT Date: **23.01.2020**

CoreEL Technologoies (I) Pvt. Ltd
21, 1st Block, 7th Main
Koramangala
Bangalore – 560 034, Karnataka

DUE DATE:07.02.2020

1. **Quotations are invited for the supply of the items as per Annexure.**
2. **The quotations duly SIGNED, SEALED AND SUPERSCRIBED ON THE ENVELOPE WITH THE REFERENCE No. AND DUE DATE,** should be addressed to the undersigned so as to reach on or before the due date stipulated above. Quotations received after the due date will not be considered.
3. The quotations should be valid for acceptance for a period of **sixty days** from the due date
4. Quotations will not be accepted by Fax, Email or any such electronic data transfer form.
5. The quotations should be for goods exactly conforming to our requirements and specifications.
6. ~~If the item is under DGS&D Rate contract, the number and the price applicable must be mentioned. It may also please be indicated whether the supply can be made direct to us at the DGS&D Rate Contract Price.~~
7. Relevant literature pertaining to the items quoted with full specifications and drawings, if any should be sent along with the quotations, wherever applicable. Samples, if called for, should be submitted free of charges and collected back at the supplier's expenses.
8. Copy of Manufacturing licence, Principal or **Authorized Distributor/Dealer Certificate, and Proprietary Certificate, as applicable**, should be enclosed.
9. Quotations should be for **free delivery** at our Centre and should clearly specify the **delivery period**. If delivery quoted is Ex-Godown/Consignor Station, delivery charges consisting of freight, packing & forwarding charges, insurance, etc. should be indicated separately. Goods should be supplied duly carriage paid and insured.
10. GST Registration Number of NIELIT Calicut is: **32AAATD0315M1Z6**. GST or any other taxes may be charged as per the rates applicable to Scientific/Educational institutions.
11. Security Deposit @ 5% of the Purchase Order/Invoice value shall be retained, in case order/contract value exceeds Rs.1 lakh, which will be released after the expiry of warranty period.
12. Goods shall not be supplied without an official purchase order.
13. Payment : Payment will be made after completion of supply, installation/assembly and commissioning of the items covered by the order along with necessary spares supplied to the entire satisfaction of NIELIT CALICUT. Payment against invoices shall normally be made within 30 days of receipt and acceptance of equipment/materials at our office. **No advance payment will be made under any circumstance**.
14. Incomplete quotations and quotations which do not comply with all the above instructions are liable to be summarily rejected.
15. NIELIT CALICUT does not bind itself to accept the lowest or any such quotation and has the right to accept or reject whole or any part of tenders or a portion of the supply of goods without assigning any reasons. No correspondence in case of rejected tenders will be entertained.
16. ~~**Earnest Money Deposit (E.M.D.) for Rs. _____/- be deposited by NEFT in the Bank Account No. 10401158037 (IFSC: SBIN0002207) at State Bank of India, NIT Calicut Branch, CREC Campus, Chathamangalam, Calicut – 673 601, in favour of Director, NIELIT CALICUT, failing which the quotation will be rejected. Proof of Deposit of EMD amount with Tenderer's Bank Account No. and IFSC No. should be submitted with the Quotation.**~~

Yours faithfully,

Purchase In-Charge
For Executive Director

Encl: **Annexure**

ANNEXURE TO ENQUIRY

Your Quotation No. Date:

1	Name of item(s)	1) Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit – **Qty. -1 No.** 2) Xilinix Zynq UltraScale+MPSoC ZCU102 Evaluation Kit – **Qty. -1 No.**
2	***Specifications & Quantity*** **As per Specifications attached.**	
3	Price per unit in Rs. (in figures & words)	Attach separate list, if required.
4	Total Price in Rupees (in figures & words)	
5	Delivery Period	
6	Terms of Delivery	
7	Taxes, Duties, Octroi & any other statutory levies or charges	
8	Transportation, Insurance, Packing & Forwarding etc.	
9	Discount/off etc., if any	
10	GST Registration No.	
11	Payment Terms	
12	Validity of Tender	
13	Warranty	
14	Any other remarks / EMD Amount and Payment details	
15	Signature of the Tenderer with Name and Date	
16	Address with Email ID & Mobile No.	
17	Central Public Procurement Portal (www.eprocure.gov.in) Registration, Email login ID	

NB: (1) The prices quoted and Taxes charged should be Academic/Educational Prices/rates, wherever applicable.

(2) Enquiry for the above items and specifications can also be downloaded from our website *http://nielit.gov.in/calicut* or *www.eprocure.gov.in*

(3) Please register at www.eprocure.gov.in and intimate login details without fail. Watch website for regular updates.

Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit

Overview:

Product Description

The Kintex® UltraScale™ FPGA KCU105 Evaluation Kit is the perfect development environment for evaluating the cutting edge Kintex UltraScale All Programmable FPGAs. The Kintex UltraScale family delivers ASIC-class system-level performance, clock management, and power management for next generation systems at the right balance of price, performance and power.

This kit is ideal for those prototyping for medium- to high-volume applications, such as Data Center, wireless infrastructure, and other DSP-intensive applications.

Key Features & Benefits

- Optimized for quickly prototyping applications using Kintex UltraScale FPGAs with access to the following features
  - 64-bit DDR4 Component Memory
  - Dual SFP+ cages for Ethernet
  - PCIe Gen3 x8
  - 2x FPGA Mezzanine Card (FMC) interface for I/O expansion

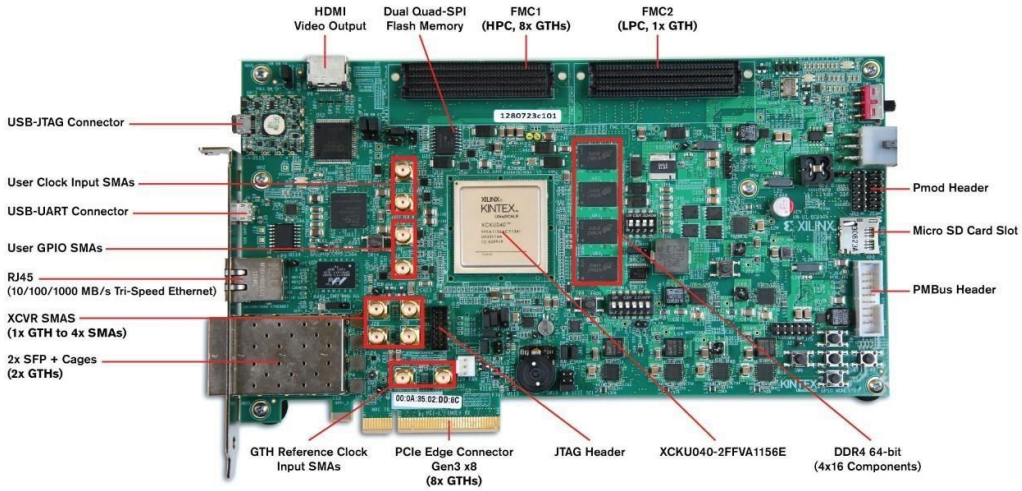
What's Included

- KCU105 evaluation board featuring the Kintex UltraScale XCKU040-2FFVA1156E FPGA
- 2x 10Gbps SFP+ modules
- 1x Fiber optic patch cable
- 1x FMC loopback card
- Access to a full seat of Vivado® Design Suite: Design Edition
  - Device-locked to the XCKU040
- Access to targeted reference designs for Ethernet, PCIe and more.
- Access to design examples for testing all major interfaces on the board.

Featured Documents

- KCU105 Quick Start Guide

Hardware:



Key Features

FPGA: Kintex XCKU040-2FFVA1156E FPGA

- ROHS compliant KCU105 kit including the XCKU040-2FFVA1156E FPGA

Configuration

- Onboard JTAG configuration circuitry to enable configuration over USB
- JTAG header provided for use with Xilinx download cables such as the Platform Cable USB II
- Quad SPI Flash with 2 x 256 Mb of non-volatile storage

Memory

- 2GB DDR4 component memory (four [256 Mb x 16] devices) at 1200MHz / 2400Mbpsps
- 64MB (512Mb) Quad SPI Flash
- 8Kb IIC EEPROM
- Micro SD Card Slot

Communication & Networking

- Gigabit Ethernet GMII, RGMII and SGMII
- 2x SFP / SFP+ cage
- GTX port (TX, RX) with four SMA connectors
- UART To USB Bridge
- PCI Express x8 edge connector

Display

- HDMI Video output
- External Phy/codec device driving an HDMI Connector
- 8x GPIO user LEDs

Expansion Connectors

- FMC-HPC (Partial Population) connector (8 GTX Transceiver, 114 single-ended or 57 differential (34 LA & 24 HA) user defined signals)
- FMC-LPC connector (1 GTX Transceiver, 68 single-ended or 34 differential user defined signals)
- 2x PMOD headers
- IIC

Clocking

- 8x programmable clocks

- System clocks, EMC clock, user clocks, Jitter attenuated clocks
- 2x SMA input clocks

Control & I/O

- 5X Directional Push Buttons
- 4X DIP Switches
- 1x Rotary switch
- Diff Pair I/O (1 SMA pair)

Power

- 12V wall adapter or ATX

Featured Components

Provider Name	Product Category	Item	Description
Maxim Integrated	Power	MAX20751 Multiphase Master with PMBus VT1697SB High Density Synchronous Buck Converter with PMBus MAX15301 InTune Digital PoL Controller MAX15303 Digital PoL with InTune Automatic Compensation MAX8869 1A Microcap LDO MAX16050/MAX16052Voltage Sequencer/Monitor ICs MAX17502 Himalaya 60V Buck Converter MAX15027 Low Voltage LDO with BIAS Input	Power semiconductors used on the KCU105 base board. More info available from Maxim's FPGA power design page

KCU105 Peripherals

- 2x 10Gbps SFP+ modules
- 1x Fiber optic patch cable

Included in this Kit

Design Tools

Name	Description	License Type
Vivado Design Suite: Design Edition	The Xilinx Vivado® Design Suite is a revolutionary IP and System Centric design environment built from the ground up to accelerate the design for all programmable devices.	Node locked & device-locked to the Kintex UltraScale KU040 FPGA, with 1 year of updates

Intellectual Property

Name	Description	License Type
PCI Express DMA Bridge Core	Northwest Logic's PCIe Expresso DMA Bridge Core	12 hour hardware time out version of the core
Memory Interface Generator (MIG)	MIG is a free software tool used to generate memory controllers and interfaces for Xilinx FPGAs	No-Charge IP

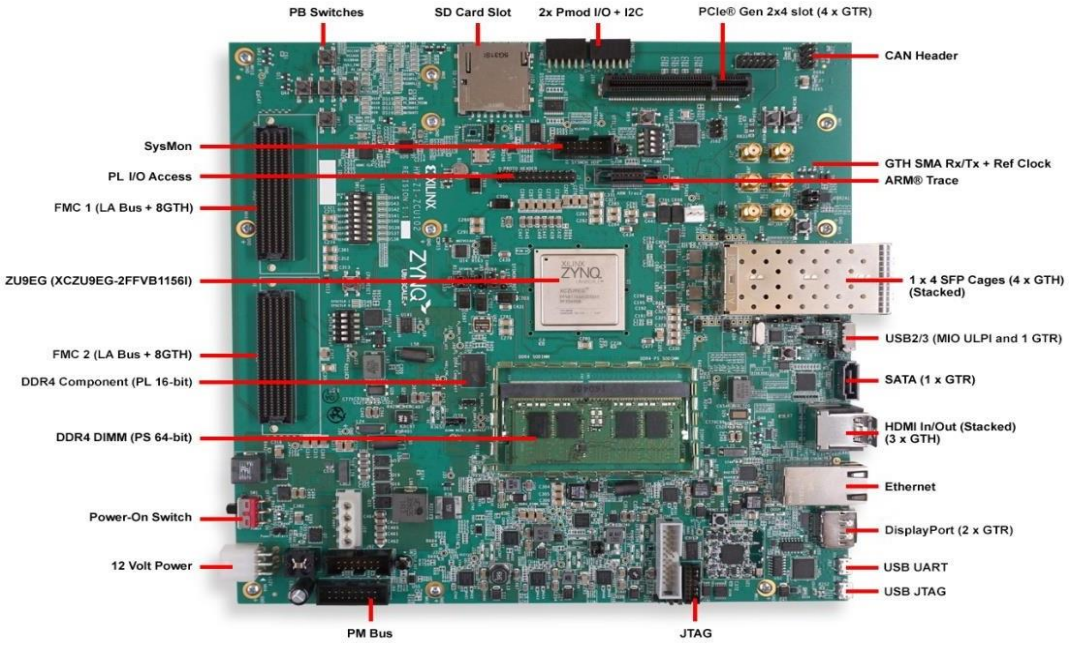
Additional Tools, IP and Resources

Provider Name	Product Category	Item	Description
Red Hat	Operating System	Fedora	Fedora-20 is used for UltraScale TRDs
Open Source	Software Tool	TeraTerm	One of many possible terminal emulators used for serial connection from your PC to the evaluation kit.

Xilinx Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit

PRODUCT DESCRIPTION

The ZCU102 Evaluation Kit enables designers to jumpstart designs for Automotive, Industrial, Video and Communications applications. This kit features a Zynq UltraScale+™ MPSoC device with a quad-core ARM® Cortex-A53, dual-core Cortex-R5 real-time processors, and a Mali-400 MP2 graphics processing unit based on Xilinx's 16nm FinFET+ programmable logic fabric. The ZCU102 supports all major peripherals and interfaces enabling development for a wide range of applications..



KEY FEATURES

- XCZU9EG-2FFVB1156I MPSoC
- PL V CCINT for range in datasheet
- Form factor for PCIe Gen2x4 Host, Micro-ATX chassis footprint
- Configuration from QSPI
- Configuration from SD card
- Configuration over JTAG with PC4 header
- Configuration over JTAG with ARM 20-pin header
- Configuration over USB-to-JTAG Bridge

- Clocks (PL-system, PS_CLK, Programmable
- Clock, SMA, SMA_GT_REF, Ethernet, USB)
- PS DDR4 64-bit SODIMM w/ ECC
- PL DDR4 Component (16-bit)
- PS GTR assignment
- SATA
- DisplayPort
- USB3
- PCIe Gen2x4 Root Port
- PL GTH assignment
- FMC #1 (8 GTH) and FMC #2 (8 GTH) PL GT assignment
- HDMI (3 GTH) PL GT assignment
- SFP+ (4 GTH) PL GT assignment
- SMA (1 GTH) PL GT assignment
- PL FMC HPC #1 Connectivity - Full LA Bus
- PL FMC HPC #2 Connectivity - Partial LA Bus
- PS MIO: QSPI
- PS MIO: Ethernet
- PS MIO: USB2 (same connector as USB3)
- S MIO: CAN
- PS MIO: UART (using USB-to-UART bridge)
- PS MIO: Second UART
- PS MIO: I2C shared across PS and PL
- PS/PL EMIO: Trace
- PL-side UART
- PL-side LEDs (8)
- PL-side DIP switch (8-position)
- PL-side Pushbuttons (5)
- PS-side Pushbutton (1)
- PS-side LED (1)
- System User Switches (PROG, CPU Reset)
- PJTAG
- Security - PSBATT button battery backup
- SYSMON
- Operational Switches (Power on/off, PROG, Boot mode)
- Operational Status LEDs (power supply status, INIT, DONE, PG, JTAG status, DDR

APPLICATIONS

- **Markets:** Industrial, Telecom / Datacom, **Medical**, Industrial, Military / Aerospace
- **Applications:** Data Transmission and Manipulation, Serial Connectivity, Digital Video, Bus Interface, High Speed Design, GPU specific

REFERENCE DESIGNS

- Embedded Applications with ARM Cortex A9 SOC.
- Video & Image processing with video FMC board & On-semiconductor Image sensor
- High Speed Transeiver Applications
- AMS evaluator Installer
- GTX IBERT design
- MIG design
- Zynq UltraScale+ MPSoC