रा.इ.सू.प्रौ.सं
NIELIT

राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान
NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY

(आई एस ओ 9001:2015 प्रमाणित) (ISO 9001:2015 CERTIFIED)
(इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय, भारत सरकार की एक स्वायत्त वैज्ञानिक संस्था)
(Autonomous Scientific Society of Ministry of Electronics and Information Technology, Government of India)
पी.बी. नं. 5, एन.आई.टी. कैम्पस पोस्ट, कालिकट - 673601, केरल, भारत P.B. No. 5, NIT Campus Post, Calicut-673 601, KERALA, INDIA
Phone : (0495) 2287266, Web : http/nielit.gov.in/calicut

Ref.No.16(70)/2023/C2S/FPGA 25-08-2023

To

Sir

Sub: Request for Quotation to Purchase of FPGA Boards and associated Design Software Tools and Installation on Proprietary Article Certificate (PAC) basis: Reg.

NIELIT Calicut is assigned centralised procurement of FPGA Boards and associated Design Software Tools under the project "Chips to Start up" (C2S) an umbrella programme of Ministry of Electronic and Information Technology (MeitY), Government fo India implemented with 100 -120 participating Academic Institutions and R&D organisation across the country.

Under this project, NIELIT Calicut intends to procure FPGA Boards and associated Design Software Tools as per attached schedule of requirements. In this regard, you are requested to send us your lowest offer/quotation along with your Original Manufacturers Company Proprietary Article Certificate and OEM Sole Authorization Certificate along with undertaking for upgrade and update for 63months from the date of installation and commissioning, on or before 12-09-2023. The detailed tender terms and conditions is also attached herewith for your compliance. You may also send us attached Annexures documents duly signed and sealed by your authorised person.

.

Purchase In-charge
for Director

Enclosed:

(1) Terms and Conditions
(2) Annexures and forms.

Annexure-II(A)

S. No	Product Name	Part Number	Product Description	Description	Specifications
1	Pynq Z2	1M1-M000127DVA	PYNQ- Python Productivity for Zynq	PYNQ- Python Productivity Board for Zynq SoC with ARM Cortex Microprocessor core for electronic systems	• FPGA Kit - Zynq-7000 SoC XC7Z020-1CLG400C - Dual ARM® Cortex™-A9 MPCore™ with CoreSight™ • I/O Interfaces: - USB-JTAG Programming circuitry - USB OTG 2.0 and USB-UART bridge - One 10/100/1G Ethernet - HDMI Input & Output - I2S interface with 24bit DAC with 3.5mm TRRS jack, Line-in with 3.5mm jack • Memory: - 512 MB DDR3 with 16-bit bus @ 1050 Mbps - 128 Mbit Quad-SPI Flash and Micro SD card connector • Switches and LEDs: - 2-Slide switches - 2-RGB LEDs - 4-LEDs - 4-Pushbuttons • Clocks: One 125 MHz for PL and One 50 MHz for PS • Expansion ports: - 2-Pmod ports (16 Total FPGA I/O) - 1-Arduino Shield connector (24 Total FPGA I/O) - Raspberry Pi connector (28 Total FPGA I/O)
2	Pmod KYPD: 16-button Keypad	410-195	PMOD	16-button keypad arranged in a hexidecimal format	• 16 momentary push-buttons • Should detect simultaneous button presses • Isolated rows and columns • Small PCB size for flexible designs 3.4"× 2.7" (8.6cm × 6.9cm) • 12-pin Pmod connector with GPIO interface
	[illegible]			Pmod OLEDrgb features a	• 96×64 pixel RGB OLED screen • 0.8" x 0.5" graphical display

3	Pmod OLEDrgb: 96 x 64 RGB OLED Display Pmod	410-323	PMOD	96 x 64 pixel RGB OLED display that is capable of 16-bit color resolution.	• 16-bit color resolution • Two low-power display shutdown modes • Small PCB size for flexible designs (1.4" x 1.0") • 12-pin Pmod connector with SPI interface
4	Pmod DA2: Two 12-bit D/A Outputs	410-113	PMOD	Pmod DA2 is a 12-bit Digital-to-Analog converter powered by the Texas Instruments DAC121S101	• 12-bit digital-to-analog converter • Two simultaneous conversion channels • Very low power consumption • Small PCB size for flexible designs 1.0"× 0.8" (2.5cm × 2.0cm) • 6-pin Pmod connector with GPIO interface
5	Pmod TPH2: 12-pin Test Point Header	410-135	PMOD	Pmod TPH2 offers 12 external pin headers for GPIO signals	• 12 external test point headers • Easily access and test signals passing through • Small PCB size for flexible designs 1.3"× 0.8" (3.3cm × 2.0cm) • 12-pin Pmod connector with GPIO interface • Follows Digilent Pmod Interface Specification Type *1*
6	Boolean Board	Boolean Board	FPGA Development Board	Educational platform built around a Xilinx Spartan-7 FPGA with peripherals and ports for stand alone designs	• FPGA Kit •I/O Interfaces: - USB-UART for programming and serial communication, - HDMI output and On-board Bluetooth Low Energy radio (option) •Memory: 128 Mbit Serial Flash •Displays: - Two 4-digit 7-Segment displays - HDMI source (up to 1080p) Audio: Two identical channels connected to 1/8" stereo audio jack • Switches and LED's: - 16 Slide switches - 16 LED's - 4 Pushbuttons • Clocks: One 100 MHz crystal oscillator • Expansion ports: - 10K Potentiometer connected to XADC - 4 - Pmod ports • Additional Features: Four servo connectors
					• FPGA Kit •I/O Interfaces: - USB-UART for programming and serial communication,

7	Urbana Board	Boolean Urbana Board	Xilinx Spartan-7 FPGA Development Board	Educational platform with Xilinx Spartan-7 FPGA platform for teaching digital design	- HDMI output and On-board Bluetooth Low Energy radio (option) •Memory: 128 MB (16b) DDR3 RAM •Displays: - Two 4-digit 7-Segment displays - HDMI source (up to 1080p) Audio: Two identical channels connected to 1/8" stereo audio jack • Switches and LED's: - 16 Slide switches - 16 LED's - 4 Pushbuttons • Clocks: One 100 MHz crystal oscillator • Expansion ports: - 10K Potentiometer connected to XADC - 4 - Pmod ports • Additional Features: Four servo connectors
8	Arty A7-100T	471-050	Artix-7 development platform	FPGA platform for MicroBlaze Soft Processing system with advanced communication protocols and PMODS.	• FPGA Kit: - Logic Cells - 101,440 - DSP Slices – 240 - Memory (Kbits) - 4,860 - GTP 6.6GB/s Transceivers – 8 - I/O Slices – 300 - Internal clock speeds exceeding 450MHz, On-chip analog-to-digital converter (XADC) and Programmable over JTAG and Quad-SPI Flash • System: - 256MB DDR3L with a 16-bit bus @ 667MHz - 16MB Quad-SPI Flash - USB-JTAG Programming circuitry (Micro B USB cable required) and Powered from USB or any 7V-15V source •Connectivity: - 10/100 Mbps Ethernet - USB-UART Bridge • Switches & LED's: - 4-Switches - 4-Buttons 1-Reset Button - 4-LEDs, 4 RGB LEDs

					• Expansion Ports: - 4 Pmod connectors Arduino/chipKIT Shield connector
9	KRIA KR260 Board	SK-KR260-G	Development platform for Kria K26 SOMs	Kria KR260 Robotics Starter Kit for robotics and factory automation applications	• FPGA Kit - System logic cells: 256K - Block RAM blocks: 144 - UltraRAM blocks: 64 - DSP slices: 1.2K • Form factor: SOM + Carrier Card + Thermal Solution • Starter kit dimensions: 119mm x 140mm x 36mm • Thermal cooling solution: Active (Fan + Heatsink) • Ethernet interface: - 4x 10/100/1000 Mb/s RJ-45s - 1x SFP+ Cage • Memory: - 4GB (4 x 512Mb x 16 bit) [non-ECC] DDR4 DDR memory - 512Mb QSPI Primary boot memory - SDHC card Secondary boot memory • Device Security: support secure boot. Infineon TPM2.0 in support of measured boot. • Interface: - Video: 1- SLVS-EC Gen2 x2 lane interface - DisplayPort 1.2a Output for 1920 x 1080 at 60Hz - I/O expansion: 4 - Pmod 12-pin interface - 1-Raspberry Pi HAT header with 26 I/Os - 4 - USB3.0/2.0 interfaces
					• FPGA Kit - System logic cells: 256K - Block RAM blocks: 144 - UltraRAM blocks: 64 - DSP slices: 1.2K • Form factor: SOM + Carrier Card + Thermal Solution • Starter kit dimensions: 119mm x 140mm x 36mm • Thermal cooling solution: Active (Fan + Heatsink) • Ethernet interface: One 10/100/1000 Mb/s

10	KRIA KV260 w/ accessory kit	SK-KV260-G+HW-BACCP01-	Kria KV260 Vision AI Starter Kit	KV260 starter kit for advanced vision application development	• Memory: - 4GB (4 x 512Mb x 16 bit) [non-ECC] DDR memory - 512Mb QSPI Primary boot memory - SDHC card Secondary boot memory • Device Security: Zynq UltraScale+ MPSoC hardware root of trust (RoT) in support of secure boot. Infineon TPM2.0 in support of measured boot. • Image sensor processor: OnSemi AP1302 ISP • Interfaces: - 2 - IAS MIPI sensor interfaces - 1 - Raspberry Pi camera interface - 1 - Pmod 12-pin interface - 4 - USB3.0/2.0 interface - 1 - DisplayPort 1.2a - 1 - HDMI 1.4
11	PYNQ-ZU development board	2M1-M00009300G	PYNQ- Python Productivity for Zynq	PYNQ- Python Productivity Board for Zynq UltraScale MPSoC with programmable logic and microprocessors for electronic systems	• FPGA - 64-bit Quadcore ARM Cortex-A53 Processors - Dualcore ARM Cortex-R5 Real-Time Processors - ARM Mali™-400MP Graphics Processor • I/O Interfaces: - Micro USB-JTAG Programming circuitry - USB 3.0 OTG PHY (supports host only) - Micro USB-UART bridge - USB Composite 3.0 - 4x USB 3.0 - HDMI 2.0 sink port (input) - HDMI 2.0 source port (output) - Mini Display Port - Audio Codec - XADC - Wifi + Bluetooth • Memory: - 4GB DDR4 2400R (64 bits wide) - Micro SD slot • Switches and LEDs: - 4 push-buttons

					- 4 slide switches - 4 LEDs - 2 RGB LEDs • Clocks - PL clock 125MHz - PL User clock 156.25 MHz - Display Port Clock 27 MHz - USB 3.0 Clock 26 MHz - PS Clock 33.333MHz • Expansion ports: - 2 standard Pmod ports and 1 TPM Pmod - MIPI CSI - FMC LPC - 40-pin Raspberry Pi connector - 3x Grove - Dual SYZYG/Y Interfaces
12	Zynq UltraScale+ MPSoC ZCU104	EK-U1-ZCU104-G	ZCU104 FPGA and MCU/MPU Evaluation Kit	Zynq UltraScale+ MPSoC ZCU104 evaluation kit with Zynq Ultrascale+ MPSoC EV device and ZU7EV device having quad-core ARM cortex for embedded Vision applications	• FPGA Kit: - System Logic Cells (K): 504 - Memory: 38Mb - DSP Slices: 1,728 - Video Codec Unit: 1 - Maximum I/O Pins: 464 • Configuration: - USB-JTAG FT4232H - Dual Quad-SPI flash memory - MicroSD Card • Memory: - PS DDR4 64-bit Component - Quad-SPI flash - Micro SD card slot • Control & I/O - 4x directional pushbuttons - DIP switches - PMBUS, clocks, and I2C bus switching - USB2/3 • Expansion Connectors

				closure,Hardware Debug and Implementation.	- CPM5 x86 host drivers for Linux and DPDK - Improved performance in QDMA v5.0 • **Wired** - DCMAC, HSC, QSGMII production on versal premium - Versal 400G RS-FEC with hard Interlaken on MRMAC FEC • **Wireless** - RFSoC DFE IP- New FT PRACH IP, Updated PRACH IP for multiband, Eval tool EoU enhancements - ORAN-PL resource reduction for Macro/Small cell - Enhancement multiband support • **Memory** - Versal HBMZE Public Access - HBM2E System C simulation • **Infrastructure, Embedded, GT Wizards** - ECC enablement on soft CAN and AXI Stream FIFO • **Multimedia** - DisplayPort 2.1 Tx - HDMI 2.1 Compliance on ZU+ - MPI CSI RX IP and DSP IP Enhancements - New MIPI CSI -2 RX example design on VEK280 - VDU General Access
				Vitis Model composer for	Model-based design tool that enables rapid design exploration within the MathWorks MATLAB® and Simulink® environment and accelerates the path to production on AMD devices through automatic code generation. Ability to design DSP algorithms and iterate through them using high-level, performance-optimized blocks and validate functional correctness through system-level simulations and improve implementation through automatic optimizations. The tool library of more than 200 HDL, HLS, and AI Engine blocks for the design and implementation of algorithms on AMD devices. Enable importing custom HDL, HLS, and AI Engine code as blocks into the tool. • Analysis, Debugging & Visualization - Use optimized AI Engine, HLS, and HDL blocks directly from the Simulink library browser. - Import custom AI Engines, HLS, and HDL code as blocks.

					- FMC LPC (1x GTH) - 3 PMOD connectors - PL DDR4 SODIMM Connector – 64 bit • Communication & Networking - USB-UARTs with FT4232H JTAG/3xUART Bridge - RJ-45 Ethernet connector - SATA (M.2) for SSD access • Display: - HDMI 2.0 video input and output (3x GTH) - DisplayPort (2x GTR) • Clocking - Programmable clocks, System clock, user clock - Jitter attenuator
13	UEF-VIVADO-ENTER-25 (2 bundles)	VIVADO Software	Vivado ML Enterprise Edition Software	FPGA Design Tool which supports Xilinx devices with inbuilt Synthesis,timing closure Hardware Debug	• **Device Support** - Devices that are production-ready - All Devices • **Simulation** - Code Coverage Support - Updated simulation tools for 3rd party tools - Enhanced support for export simulation flow • **Implementation & Synthesis** - Bitstream generation via multithreading – Extending support for Versal - Flexible MARK_DEBUG Processing during PnR - New Post-Placement Physical Optimizations - VHDL-2019 Support • **Timing Closure** - Intelligent Design Run (IDR) improvements – For Versal and UltraScale+ Designs - Report QoR Assessment (RQA) enhancements • **Hardware Debug** - BSCAN Fallback for AXI Debug Hub for Versal - DFX Debug Support for 'Insertion' Flow – Versal • **PCIE subsystems**

14	UEF-MATSIM-ADDON-25 (2 bundles)	Matsim Addon software	Vitis Model Composer Software	Vitis Model Composer for model-based design for design exploration within MATLAB and Simulink environment	- Run fast simulations in the Simulink environment. - Compare the results with golden references in the MATLAB and Simulink environment. - Tap into intermediate signals to debug and get visibility into the design. • Co-Simulation of AI Engines and Adaptable Engines - Directly use optimized AI Engines/HLS/Adaptable Engines from the library browser or import code as blocks - Seamlessly connect AI Engine arrays with HLS kernel blocks or HDL blocks • Code Generation - Generate graph code along with constraints - Generate RTL (Verilog/VHDL) - Generate optimized HLS code with inserted pragmas - Generate a test bench • Validation of Design in Hardware - Generate data movers, processing system code, config files - Generate the make files to build the design for hardware - Move the design into hardware with a click of a button
15	VCK5000 Versal Development Card	DK-VCK5000-G-ED	Xilinx VCK5000 Versal Development Card	AMD VCK 5000 Versal Development Card server class development platform for Cloud acceleration and Edge computing applications with fully supported Vitis AI development environment.	• Device: VC1902 • Compute: Active • INT8 TOPs (peak): 145 • Dimensions - Height: Full - Length: Full - Width: Dual Slot • Memory - Off-chip Memory Capacity: 16 GB - Off-chip Total Bandwidth: 102.4 GB/s - Internal SRAM Capacity: 23.9 MB - Internal SRAM Total Bandwidth: 23.5 TB/s • Interfaces - PCI Express: Gen3 x 16 / Gen4 x 8 - Network Interfaces: 2x QSFP28 (100GbE) • Logic Resources: Look-up Tables (LUTs) - 899,840 • Power and Thermal

					- Maximum Total Power: 225W - Thermal Cooling: Active
16	Alveo U55C	A-U55C-P00G-PQ-G	Xilinx® Alveo™ U55C high performance compute card	ALVEO U55C high performance card high speed accelerator for high performance computing	• Compute Resources - Look-up Tables (LUTs): 1,304K - Registers: 2,607K - DSP Slices: 9,024 • Dimensions - Height: Full Height - Length: Half Length - Width: Single Slot • Memory - HBM Memory Capacity: 16 GB - HBM Total Bandwidth: 460 GB/s - Internal SRAM Capacity: 43 MB - Internal SRAM Total Bandwidth: 35 TB/s • Physical Interfaces: - PCI Express: Gen3x 16, 2 x Gen4x 8 • Network Interfaces: 2x QSFP28 • Tool Support: Vitis Developer Environment • Platforms - Vitis Unified Software Platform: Gen3x16 XDMA - Vivado Design Suite • Power and Thermal - Maximum Total Power: 150W - Typical Power: 115W - Thermal Cooling: Passive • Target Workloads: Big data analytics and search, financial computing, computational storage, and machine learning
					• **Device Support** - Devices that are production-ready - All Devices • **Simulation** - Code Coverage Support - Updated simulation tools for 3rd party tools - Enhanced support for export simulation flow

17	UEF-VIVADO-ENTER-25 (2 bundles)	VIVADO Software	Vivado ML Enterprise Edition Software	FPGA Design Tool supporting Xilinx devices with inbuilt Synthesis,timing closure,Hardware Debug and Implementation.	• **Implementation & Synthesis** - Bitstream generation via multithreading – Extending support for Versal - Flexible MARK_DEBUG Processing during PnR - New Post-Placement Physical Optimizations - VHDL-2019 Support • **Timing Closure** - Intelligent Design Run (IDR) improvements – For Versal and UltraScale+ Designs - Report QoR Assessment (RQA) enhancements • **Hardware Debug** - BSCAN Fallback for AXI Debug Hub for Versal - DFX Debug Support for 'Insertion' Flow – Versal • **PCIE subsystems** - CPM5 x86 host drivers for Linux and DPDK - Improved performance in QDMA v5.0 • **Wired** - DCMAC, HSC, QSGMII production on versal premium - Versal 400G RS-FEC with hard Interlaken on MRMAC FEC • **Wireless** - RFSoC DFE IP- New FT PRACH IP, Updated PRACH IP for multiband, Eval tool EoU enhancements - ORAN-PL resource reduction for Macro/Small cell - Enhancement multiband support • **Memory** - Versal HBMZE Public Access - HBM2E System C simulation • **Infrastructure, Embedded, GT Wizards** - ECC enablement on soft CAN and AXI Stream FIFO • **Multimedia** - DisplayPort 2.1 Tx - HDMI 2.1 Compliance on ZU+ - MPI CSI RX IP and DSP IP Enhancements - New MIPI CSI -2 RX example design on VEK280 - VDU General Access

18	UEF-MATSIM-ADDON-2	Matsim Addonn software	Vitis Model Composer Software	Vitis Model composer for model-based design for design exploration within MATLAB nd Simulink environment	Model-based design tool that enables rapid design exploration within the MathWorks MATLAB® and Simulink® environment and accelerates the path to production on AMD devices through automatic code generation. Ability to design DSP algorithms and iterate through them using high-level, performance-optimized blocks and validate functional correctness through system-level simulations and improve implementation through automatic optimizations. The tool library of more than 200 HDL, HLS, and AI Engine blocks for the design and implementation of algorithms on AMD devices. Enable importing custom HDL, HLS, and AI Engine code as blocks into the tool. Analysis, Debugging & Visualization - Use optimized AI Engine, HLS, and HDL blocks directly from the Simulink library browser - Import custom AI Engines, HLS, and HDL code as blocks - Run fast simulations in the Simulink environment - Compare the results with golden references in the MATLAB and Simulink environment - Tap into intermediate signals to debug and get visibility into the design Co-Simulation of AI Engines and Adaptable Engines - Directly use optimized AI Engines/HLS/Adaptable Engines from the library browser or import code as blocks - Seamlessly connect AI Engine arrays with HLS kernel blocks or HDL blocks Code Generation - Generate graph code along with constraints - Generate RTL (Verilog/VHDL) - Generate optimized HLS code with inserted pragmas - Generate a test bench Validation of Design in Hardware - Generate data movers, processing system code, config files - Generate the make files to build the design for hardware - Move the design into hardware with a click of a button

19	101 SITES SUPPLY /SUPPORT INSTALLATION/75 DAYS OF TRAINING FOR PRODUCTS- OFF LINE /ON LINE WITH CERTIFICATES GIVEN TO ALL PARTICIPANTS FOR COMPLETION FROM AUTHORIZED TRAINING PARTNER OF AMD-XILINX /, UNLIMITED PARTICIPANTS FROM ALL INSTITUTES, /24X7 SUPPORT/, EVERY YEAR NEW SOFTWARE INSTALLATION/TECHNICAL SERVICE AND ISSUE SOLVING /5 YEARS 3 MONTHS SERVICE WARRANTY.				Software & Hardware installation (Online or On-site) at 101 institutions and User guidance - ATP Training for 25 Programs in 5 Years* - Project Support - 24 / 7 Online technical assistance *ATP Training programs - 5 Programs per Year at selected nodal / regional centres. Each program would be for 3 days, cumulating to 15 Days of training program per year and a total of 75 training days in 5 Years.* *Each day constitute 6 hours of training and 30% should be theory / concepts and 70% hands-on training.*

Annexure-II(B)

Compliance Sheet

Terms and Conditions	Compliance/Remarks
1. Number of academic-research institutions under Chip-to-Startup (C2S) Programme that will use FPGA boards and associated software tools: 100 to 120. Presently, 100 institutes are being considered.	
2. List of participating institutes and the centralized site with the details of Principal Investigator (PI) and Co-Principal Investigator (Co-PI) will be provided to the vendor for execution of the purchase order. ➢ It is possible that at the time of issuing the purchase order, a limited number of participating institutes (marginally less than 100) would be identified and the same would be conveyed to the vendor. ➢ Subsequent addition of participating institutes would be communicated from time-to-time to the vendor.	

3. Institutions can be removed/added (maximum up to 120) throughout the duration of the 5 years and 3 months (buffer period for on-boarding participating institutes) without any further financial implications. ➢ Participating institutes (based on available financial funds with them) can order additional hardware items (FPGA boards or kits) at the same rates within 9 months from the list of items in the original centralized procurement order. ➢ If additional hardware (FPGA boards or kits) or software (FPGA design tools) for more than 100 institutions are required to procured within 9 months from the original centralized procurement order, it will be done via centralized procurement on pro-rata basis without any need for a fresh quotation. ➢ Procurement to support additional institutes (beyond 100 nos. of institutes) and beyond 9 months from original centralized procurement will require fresh negotiation and quotation.	
4. Each participating institution will sign the necessary end-user agreement to enable the FPGA design software licenses and confirm their academic/educational/research usage.	
5. Some high-end FPGA boards, identified by the CEPC, will be hosted at centralized site (C-DAC, Bengaluru). There will be a provision to remotely (or physically) access these high-end FPGA boards by the participating institutions.	
Warranty, Support, and Updates/Upgrades:	

6. Vendor should provide onsite warranty for the FPGA boards for a period of 90/120/180/365 days as indicated by the OEM or the supplier. However, technical support services for the FPGA boards need to be provided for the entire duration of 5 years and 3 months.	
7. Vendor should provide requisite upgrades and updates for all associated FPGA design software tools for the duration of 5 years and 3 months.	
8. Warranty/support period's start date shall be from the date of installation/commissioning of the items and acceptance at the participating institute.	
Support and Online Training:	
9. Vendor needs to provide support login and website access details for two persons per participating institution and two persons for the programme coordinating site at C-DAC, Bengaluru. ➢ Support login should provide access to online recorded videos, tutorials, tool-flow documents, white-papers, user-guides, technical support to queries, forums, etc.	

3. Institutions can be removed/added (maximum up to 120) throughout the duration of the 5 years and 3 months (buffer period for on-boarding participating institutes) without any further financial implications. ➢ Participating institutes (based on available financial funds with them) can order additional hardware items (FPGA boards or kits) at the same rates within 9 months from the list of items in the original centralized procurement order. ➢ If additional hardware (FPGA boards or kits) or software (FPGA design tools) for more than 100 institutions are required to procured within 9 months from the original centralized procurement order, it will be done via centralized procurement on pro-rata basis without any need for a fresh quotation. ➢ Procurement to support additional institutes (beyond 100 nos. of institutes) and beyond 9 months from original centralized procurement will require fresh negotiation and quotation.	
4. Each participating institution will sign the necessary end-user agreement to enable the FPGA design software licenses and confirm their academic/educational/research usage.	
5. Some high-end FPGA boards, identified by the CEPC, will be hosted at centralized site (C-DAC, Bengaluru). There will be a provision to remotely (or physically) access these high-end FPGA boards by the participating institutions.	
Warranty, Support, and Updates/Upgrades:	

10. Technical support and assistance via phone, e-mail, webinar, or online video/audio needs to be provided by the FPGA boards vendor during the entire duration of 5 years and 3 months.	
11. Vendor should share the design flow documents for FPGA design software tool (if unavailable on their support website) for any specific software tools and its features. ➢ This will be on-need basis only to ease the usage of tools for the C2S participating institutes.	
12. Badging/certification facility is not required to be provided for students for the online training materials.	
Site Preparation:	

13. The vendor shall inform to the participating institute about the site preparation, if any, needed for the installation of the FPGA boards and associated FPGA design software tools, immediately after the receipt of the purchase order. ➢ The vendor must provide complete details regarding space and all the other infrastructural requirements needed for the FPGA boards and associated FPGA design software tools, which the institute should arrange before the arrival of the FPGA boards and associated design software tools to ensure their timely installation and smooth operation thereafter. ➢ The vendor may speak with the Principal Investigator (PI) or Co-Principal Investigator (Co-PI) of the participating institute and render assistance to the institute in the preparation of the site and other pre-installation requirements.	
Installation, Commissioning, and Demonstration:	
14. Installation certificate needs to be provided after successful installation and commissioning of FPGA boards along with the associated FPGA design software tools for each site. ➢ This installation certificate will have to be duly signed and stamped along with the date by the installation engineer of the FPGA boards vendor (or its representative) and either by the Principal Investigator (PI) or by the Co-Principal Investigator (Co-PI) at each site. The certificate will also confirm if this was done via online method or by on-site visit. ➢ Installation and commissioning, i.e. one-time demonstration of the proper working of FPGA boards along with the associated FPGA design software tools, at each site has to be done by the vendor. This would be done preferably using online methods (email, phone, chat, video, audio, webinar, etc.). On-site assistance for installation and commissioning needs to be done only when specifically requested with justification by any participating institute. ➢ The vendor is required to complete the installation and demonstration of the supplied items at mutually agreed dates in consultation with PI/Co-PI at each site.	

➢ In case of any damage to FPGA boards during their transportation from the starting/staging location (from within India) to the installation site, the supplier has to replace it with new FPGA board at the earliest.	
15. On arrival of shipment/consignment, the vendor is required to arrange custom clearance and transportation of the consignment up to the participating institute premises.	
Indicative Procurement Process and Payment Terms and Conditions:	
16. Budgetary quote should separately indicate the cost and applicable GST rate and any other taxes/duties.	
17. The purchase process shall be through GeM (Government e-Marketplace). ➢ If this is not possible, the same needs to be justified by the vendor.	
18. Offers made by Indian agents (or representatives) on behalf of their principals should be supported by the necessary authorization letter from their principals.	
19. Make in India (MII) certificate shall be provided by the vendor. ➢ If not available or feasible, the same needs to be clearly mentioned.	

20. Proprietary certificate must be provided for all the boards and software design tools that have been proposed. ➢ This certificate may be addressed as "To Whomsoever It May Concern."	
21. Broad specification for all the items that have been proposed needs to be provided. ➢ The specification can be a brief write-up on the FPGA boards. ➢ The specification can be a brief write-up on the associated FPGA design software tools.	
22. Terms of Payments: The payment would be released in stages as detailed below: ➢ STAGE-1: 80% of total PO value to be released after successful installation and commissioning of the FPGA boards and associated FPGA design tool licenses at a minimum of 50 numbers of on-boarded participating institutes OR after 1 month has elapsed from the date of delivery of the FPGA boards to the staging site (starting location in India) and associated FPGA design tool licenses have been received by each of the indicated 50 numbers participating institute site (whichever is earlier). In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution. ➢ Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning.	

➢ STAGE-2: 17% of total PO value to be released after successful installation and commissioning of the FPGA boards and associated FPGA design tool licenses at the balance 50 numbers of on-boarded participating institutes OR after 2 months have elapsed from the date of delivery of the FPGA boards to the staging site (starting location in India) and associated FPGA design tool licenses have been received by each of the balance 50 numbers of participating institute site (whichever is earlier). In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution. ➢ Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning. ➢ SPECIAL-CASE: If successful installation and commissioning of FPGA boards and associated FPGA design tool licenses is completed at all the 100 numbers of on-boarded participating institutes during the first 1 month, 97% of total PO value will be released to the vendor. In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution. ➢ Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning.	
23. Performance Bank Guarantee: 3% payment of the PO value will be paid against (electronic) performance bank guarantee issued by any nationalized/scheduled bank of India valid for 5-year license period and 3-month buffer period with an additional 1-month, i.e. with 64-month validity. Other instruments in lieu of ePBG may be also permitted as per government orders issued from time-to-time for this purpose. ➢ Note that this payment of 3% against ePBG will be released along with STAGE-1 payment. ➢ If no bank guarantee (or a suitable permitted alternative) for the 3% of the PO value is provided, the balance 3% payment will be made only after expiry of 64 months.	

Annexure-2(C)

Specific Terms and Conditions for Procurement of FPGA Boards and Associated Software Tools for C2S Programme

General:

1. Number of academic-research institutions under Chip-to-Startup (C2S) Programme that will use FPGA boards and associated software tools: 100 to 120. *Presently, 100 institutes are being considered.*
2. List of participating institutes and the centralized site with the details of Principal Investigator (PI) and Co-Principal Investigator (Co-PI) will be provided to the vendor for execution of the purchase order.
   2.1. It is possible that at the time of issuing the purchase order, a limited number of participating institutes (marginally less than 100) would be identified and the same would be conveyed to the vendor.
   2.2. Subsequent addition of participating institutes would be communicated from time-to-time to the vendor.
3. Institutions can be removed/added (maximum up to 120) throughout the duration of the 5 years and 3 months (buffer period for on-boarding participating institutes) without any further financial implications.
   3.1. Participating institutes (based on available financial funds with them) can order additional hardware items (FPGA boards or kits) at the same rates within 9 months from the list of items in the original centralized procurement order.
   3.2. If additional hardware (FPGA boards or kits) or software (FPGA design tools) for more than 100 institutions are required to procured within 9 months from the original centralized procurement order, it will be done via centralized procurement on pro-rata basis without any need for a fresh quotation.
   3.3. Procurement to support additional institutes (beyond 100 nos. of institutes) and beyond 9 months from original centralized procurement will require fresh negotiation and quotation.
4. Each participating institution will sign the necessary end-user agreement to enable the FPGA design software licenses and confirm their academic/educational/research usage.
5. Some high-end FPGA boards, identified by the CEPC, will be hosted at centralized site (C-DAC, Bengaluru). There will be a provision to remotely (or physically) access these high-end FPGA boards by the participating institutions.

Warranty, Support, and Updates/Upgrades:

6. Vendor should provide onsite warranty for the FPGA boards for a period of 90/120/180/365 days as indicated by the OEM or the supplier. However, technical support services for the FPGA boards need to be provided for the entire duration of 5 years and 3 months.
7. Vendor should provide requisite upgrades and updates for all associated FPGA design software tools for the duration of 5 years and 3 months.

8. Warranty/support period's start date shall be from the date of installation/commissioning of the items and acceptance at the participating institute.

Support and Online Training:

9. Vendor needs to provide support login and website access details for two persons per participating institution and two persons for the programme coordinating site at C-DAC, Bengaluru.

    9.1. Support login should provide access to online recorded videos, tutorials, tool-flow documents, white-papers, user-guides, technical support to queries, forums, *etc.*

10. Technical support and assistance via phone, e-mail, webinar, or online video/audio needs to be provided by the FPGA boards vendor during the entire duration of 5 years and 3 months.

11. Vendor should share the design flow documents for FPGA design software tool (if unavailable on their support website) for any specific software tools and its features.

    11.1. This will be on-need basis only to ease the usage of tools for the C2S participating institutes.

12. Badging/certification facility is not required to be provided for students for the online training materials.

Site Preparation:

13. The vendor shall inform to the participating institute about the site preparation, if any, needed for the installation of the FPGA boards and associated FPGA design software tools, immediately after the receipt of the purchase order.

    13.1. The vendor must provide complete details regarding space and all the other infrastructural requirements needed for the FPGA boards and associated FPGA design software tools, which the institute should arrange before the arrival of the FPGA boards and associated design software tools to ensure their timely installation and smooth operation thereafter.

    13.2. The vendor may speak with the Principal Investigator (PI) or Co-Principal Investigator (Co-PI) of the participating institute and render assistance to the institute in the preparation of the site and other pre-installation requirements.

Installation, Commissioning, and Demonstration:

14. Installation certificate needs to be provided after successful installation and commissioning of FPGA boards along with the associated FPGA design software tools for each site.

    14.1. This installation certificate will have to be duly signed and stamped along with the date by the installation engineer of the FPGA boards vendor (or its representative) and either by the Principal Investigator (PI) or by the Co-Principal Investigator (Co-PI) at each site. The certificate will also confirm if this was done via online method or by on-site visit.

14.2. Installation and commissioning, *i.e.* one-time demonstration of the proper working of FPGA boards along with the associated FPGA design software tools, at each site has to be done by the vendor. This would be done preferably using online methods (email, phone, chat, video, audio, webinar, *etc.*). On-site assistance for installation and commissioning needs to be done only when specifically requested with justification by any participating institute.

14.3. The vendor is required to complete the installation and demonstration of the supplied items at mutually agreed dates in consultation with PI/Co-PI at each site.

14.4. In case of any damage to FPGA boards during their transportation from the starting/staging location (from within India) to the installation site, the supplier has to replace it with new FPGA board at the earliest.

Custom Clearance and Delivery:

15. On arrival of shipment/consignment, the vendor is required to arrange custom clearance and transportation of the consignment up to the participating institute premises. Supply, installation, testing and commissioning of the tools/equipment's/items covered under this requirements, at the premises of various installation sites at various locations across the country, are required to be completed in all respects.

Indicative Procurement Process and Payment Terms and Conditions:

16. Your quote should separately indicate the cost and applicable GST rate and any other taxes/duties, insurance, etc. The total price quoted must be all inclusive. The price is F.O.R. Destination/delivery locations basis.

17. Offers made by Indian agents (or representatives) on behalf of their principals should be supported by the necessary authorization letter from their principals.

18. Make in India (MII) certificate shall be provided by the vendor.

    18.1. If not available or feasible, the same needs to be clearly mentioned.

19. Proprietary certificate must be provided for all the boards and software design tools that have been proposed.

    19.1. This certificate may be addressed as "To Whomsoever It May Concern."

20. **Terms of Payments:** The payment would be released in stages as detailed below:

    20.1. **STAGE-1:** 80% of total PO value to be released after successful installation and commissioning of the FPGA boards and associated FPGA design tool licenses at a minimum of 50 numbers of on-boarded participating institutes OR after 1 month has elapsed from the date of delivery of the FPGA boards to the staging site (starting location in India) and associated FPGA design tool licenses have been received by each of the indicated 50 numbers participating institute site (whichever is earlier). In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution.

        20.1.1. Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning

20.2. **STAGE-2:** 17% of total PO value to be released after successful installation and commissioning of the FPGA boards and associated FPGA design tool licenses at the balance 50 numbers of on-boarded participating institutes OR after 2 months have elapsed from the date of delivery of the FPGA boards to the staging site (starting location in India) and associated FPGA design tool licenses have been received by each of the balance 50 numbers of participating institute site (whichever is earlier). In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution.

20.2.1. Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning.

20.3. **SPECIAL-CASE:** If successful installation and commissioning of FPGA boards and associated FPGA design tool licenses is completed at all the 100 numbers of on-boarded participating institutes during the first 1 month, 97% of total PO value will be released to the vendor. In case the installation and commissioning does not get completed due to "site not ready" reason at any participating institute, the payment to vendor will be made without any further delay or hold-up because of that institution.

20.3.1. Point nos. 13 and 14 (as applicable) of the broad terms and conditions must be satisfied for successful installation and commissioning.

21. **Performance Bank Guarantee:** 3% payment of the PO value will be paid against (electronic) performance bank guarantee issued by any nationalized/scheduled bank of India valid for 5-year license period and 3-month buffer period with an additional 60 days, *i.e.* with 65-month validity. Other instruments in lieu of ePBG may be also permitted as per government orders issued from time-to-time for this purpose.

21.1. Note that this payment of 3% against ePBG will be released along with STAGE-1 payment.

21.2. If no bank guarantee (or a suitable permitted alternative) for the 3% of the PO value is provided, the balance 3% payment will be made only after expiry of 65 months

22. Other general terms and conditions as part of the purchase process will be included in the RFQ.

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)
P.B. No.5, NIT Campus, CALICUT – 673601, KERALA

Website: www.nielit.gov.in/calicut/index.php Email: purchase@calicut.nielit.in

Our Enquiry No : No16(70)/2023/C2S/FPGA dt. 25.08.2023

GENERAL TERMS & CONDITIONS FOR SUPPLY OF PROPRIETARY ARTICLES

1) PROPRIETARY ARTICLE CERTIFICATE:- A list of items given in the Schedule of Requirement/Specifications in Annexure-II fall in the Proprietary Article Category, the Proprietary Article Certificate must be enclosed by the Original Manufacturer Company on their Official Letter head duly Signed and Stamped by the Authorized Signatory.

2) PRICE QUOTATION:- Prices for Proprietary Articles should be quoted either by the original Manufacturer or their sole Distributor/Dealer Agency existing in India in the Price Quotation format given in Annexure-III

3) AUTHORIZATION LETTER IN FAVOUR OF SOLE DISTRIBUTOR/DEALER/RESELLER:- It is the responsibility of Original Equipment Manufacturer (OEM) to give the Authorization Letter in favour of their Sole Distributor/Dealer Agency for supply/quote for requested Proprietary Articles on their Official Letter head duly signed and stamped by the Authorized Signatory of the Manufacturing Firm. Manufacturers name and country of origin of materials offered must be clearly specified.

4) VALIDITY & SUPPLY OF APPROVED ITEMS IN QTY TO ANY EXTENT:-

The Sole/Authorized reseller is responsible for the supply of Proprietary Articles as per Schedule of Requirements/Specifications to PCI(CDAC,Bangalore)/Participating Institutes (PI's) across the courny & R&D organization etc. provided by us on receipt of Purchase Order and liable to supply the ordered approved Proprietary Article on as per purchase order terms and conditions.

5) RIGHTS TO NIELIT CALICUT: - If the Principal Manufacturer withdraws rights of distribution from the Distributor/Dealer/ Reseller during validity period of contract/purchase order or before completion of supply the ordered items, the Original Manufacturer himself will be responsible for supply of the approved Proprietary Articles till the new Distributor/Dealer Agency appointed by him for the supply. Director, NIELIT Calicut has right to cancel the eligibility of the such discontinued Distributor/Dealer Agency and accept the candidature of newly coming authorized Distributor/Dealer of the Original Manufacturer on receiving official communication from his end.

6) **EMD/Bid Security Clause:** In order to avail the benefit of waiver of EMD, the seller while submitting offer/quotation Undertaking for EMD/ Bid Security Declaration as per Annexure -IV must be submitted along with your offer.

7) DEVIATION IN REQUESTED SPECIFICATIONS: - The eligible Bidder/dealer/Reseller Agency is required to quote strictly as per Schedule of Requirements/specifications as per attached Annexure-II. Any deviation in specification must be brought out clearly giving deviation statement during forwarding their proposal on separate Sheet heading "Deviations" if any.

8) The Bidder should submit an undertaking for acceptance of Terms & Conditions "Annexure-V" on his letter head duly signed by the authorized person and stamped to fulfill all the obligation mentioned here.

9) IMPORTANT POINTS FOR QUOTING PRICES: - The Bidder should also keep following points in mind during offering his techno/price quotation against this Request for Quotation Enquiry:-

(i) No increase in quoted price and change in quality of product will be allowed during the validity of the entire supply period or any extended Contract Period mutually agreed upon by the both parties (i.e. Dealer and NIELIT, Calicut).

(ii) Bidder/Dealer will quote firm rates inclusive of all Taxes & expenditure up to F.O.R. destination basis. Rates should be according to a unit e.g. cost per unit (as asked in the Schedule of Requirement i.e. Each/Kit/Item/Entire software package etc. which so ever applicable with clearly mentioning its pack size, preferably as per asked pack size) and not in any other form. Quoting of rates in variation to the prescribed unit will authorize the Competent Authority to cancel the quotation without any information to the bidder.

(iii) No item should be quoted with price more than the M.R.P. The prices should be quoted strictly in accordance with unit/quantity mentioned in the Price Quotation format.

10) FALL CLAUSE:- If at any time during the execution of the contract, the Contractor/Manufacture/Distributor/Dealer reduces the sale price or sells or offers to sell such stores, as are covered under the contract, to any person/organization including the purchaser or any department of Central Government or any other Institutions/PSUs at a price lower than the price chargeable under the contract during the Current Financial Year, he shall forthwith notify Director, NIELIT Calicut. The necessary difference amount about such reduction or sale or offer of sale to the purchaser and the price payable under the contract for the stores supplied after the date of coming into force of such reduction or sale or offer of sale shall stand correspondingly reduced and deposited to NIELIT Calicut by the Bidder or will deduct from the pending bills/Performance Guarantee (as per Annexure-VI).

11) GST Applicability: Payment of GST is primarily the responsibility of the seller and will not be paid unless the percentage value is clearly mentioned in the quotations. If no indication regarding GST is recorded in the quotation, the GST will be considered as included.

12) DELIVERY OF THE SUPPLIES/STORES & PENALTY ON DELAYED SUPPLY: -

Delivery period required for supplying the materials should be invariably specified in the quotation

(i) Rate quoted should be free delivery, installation and commissioning at FOR Destinations including all charges otherwise the quotation is likely to be rejected. If there is no indication regarding the FOR, in the quotation, then it will be considered as FOR destination. Price quoted should be net and valid for a minimum period of 3 months from the date of opening the quotation.

(ii) In case your quotation is accepted and purchase order is placed on you, the supply against the order should be made within the period stipulated in the order. If the deliveries are not maintained and due to that account NIELIT Calicut is forced to buy the material at your risk and cost from elsewhere, the loss or damage that may be sustained there by will be recovered from the defaulting supplier. The above shall be in addition to black listing of the firm depending upon the circumstances of the default/merit of the case.

(iii) The period of delivery strictly to be followed by the Supplier Agency as per time period communicated through Purchase/Supply Order through e-mail/hard copy through speed post. The penalty/LD @0.50% per week will levied on supply order value of the item and will be deducted from the payment Bill. The maximum penalty will be 10% against any of Purchase/Supply Order total value (i.e. the maximum delay acceptable only 10 weeks from the time stipulated in the Supply/Purchase Order subject to deduction of applicable LD). No supplies will be entertained after

expiry of given supply period subject to deduction of applicable LD beyond the time given in the Supply/Purchase Order from the date of issue of supply order as supply order will be treated as cancelled without any further reference and the action as deemed fit shall be initiated as per above para against such defaulter OEM/Distributor/Dealer. Wherever, installation and commissioning is also involved, the supply will be deemed to have been completed only when the entire Stores is supplied, installed and accepted

(iv) Part supplies generally will not be accepted. However, as per requirement, the vendors shall meet the urgent nature requirement immediately on part supply basis in the public interest whenever asked by NIELIT Calicut. For non-supply or part/partial supply, Penalty/LD as per applicable rate mentioned above in above para (iii) shall be imposed and deducted from the Pending Bills of the Reseller/Agency and action deemed fit shall be initiated. Seller can deposit the penalty with the Buyer directly else the Buyer shall have a right to recover all such penalty amount from the pending Invoice/Performance Security (ePBG).

13) INSPECTION AND ACCEPTANCE OF SUPPLIES:-

All supplies are subject to inspection and approval before acceptance. Inspection and Acceptance will be done by the to PCI(CDAC,Bangalore)/Participating Institutes(PI)/Organisations where supply and installation has been carried out by the Vendor/Supplier (Refer Annexure-II) upon satisfactory receipt of items as per our purchase order. Manufacturer/supplier warranty certificate shall be furnished along with supply.

Vendor should arrange to submit Installation certificates duly signed by both PI/Co-PI of the participating institute and authorized representative of the vendor to PCI (CDAC Bangalore).

14) PAYMENTS: -

No advance payment will be made under any circumstance. The Payments will be released in stages wise as per attached Schedule of Requirements/Specification Annexure-IIC. The GST/Custom Duty and any other Taxes of Statutory bodies should be included in the Payment Claim Bill of Supplier Agency and the Agency/Reseller solely will liable for necessary Tax Deposition to the concerned Statutory Tax Department as per applicable rules and NIELIT Calicut will release Claim Payment after due deduction of applicable TDS or any statutory charges on prevailing rules to Supplier Agency after satisfactory acceptance of supplied Goods/Software.

The payment will be released to the vendor only upon receipt of consolidated installation certificate from PCI (CDAC Bangalore) & installation certificates (duly signed by vendor and PI/Co-PI of the participating Institute) along with recommendation for the release of payment from *PCI (CDAC Bangalore).*

GST registration No. and date of its validity should be indicated. The firm must quote their TIN No., PAN/TAN No., etc. in the quotation (attested copies to be enclosed). The seller is requested to indicate **NIELIT Calicut GST No.32AAATD0315M1Z6** on the tax invoice.

15) PERFORMANCE SECURITY DEPOSIT:-

The Supplier Agency should deposit **3**% value of Purchase Orders as a Performance Security Deposit in favor of "Director, NIELIT Calicut" in the form of FDR/Performance Security Bank Guarantee from Scheduled National/Commercial Bank in India for the entire warranty period plus 60 days with effect from date of installation and commissioning. Performance Security will be valid upto 60 days after the date of completion of all contractual obligations by the Supplier, including the

"Defect Liability Obligations". If the Supplier/Reseller/Seller Agency does not fulfill the Contractual obligation/any breach of Contract does not honor Purchase Order of during Contract Period, the NIELIT Calicut should have full right to forfeiture of Performance Security Deposit Amount of Supplier/Seller Agency in total. The Performance Security Deposit shall be released to the Supplier Agency on successful completion of the Performance Security Deposit Period on receipt of satisfactory performance certificate from concerned User department/Institutions and also receipt of "No Dues Certificate" in the attached format from the supplier. No interest will be paid on any EMD/SD or any pending invoice amount or any payment due to supplier under any circumstance.
In case if Security Deposit is submitted and the contractor fails to execute the order, then the security deposit will be forfeited.
Alternately vendors can request for withholding **3%** payment till completion of the warranty period
SD, LD and PBG clauses are mandatory and offers of the vendors who have not agreed for the above conditions will be excluded from the procurement process. Micro and Small Vendors are not exempted from the submission of Security Deposit

16) DISPUTES AND ARBITRATION: -

All disputes or differences arising during the execution of this Contract shall be resolved by the mutual discussion failing which the matter will be referred to an Arbitrator who will appointed by the **Director of NIELIT, Calicut**, for Arbitration for settlement of disputes in accordance with Arbitration & Conciliation Act 1996 or its subsequent amendment, whose decision shall be binding on the contracting parties.

17) LAW GOVERNING THE CONTRACT and Jurisdiction
The Purchase Order shall be construed, interpreted and governed by the Laws of India. Any dispute relating to this purchase shall be subject to the jurisdiction of the court of Calicut/Kozhikode, Kerala State only.

18) Part Order/Repeat Order

The Supplier hereby agrees to accept part order at Buyer's option without any limitation whatsoever and also accept repeat order(s) during a period of six months from the date of original Purchase Order at the same unit price(s) and on the same terms and conditions as contained in the original Purchase Order. The fall clause as indicated in Sl. No.10 is also applicable in case of repeat order, if any. It will be entirely the discretion of the Buyer to exercise the repeat purchase order or not.

19) Warranty: The Supplier warrants to the Buyer that each and every equipment, its accessories etc. supplied by the Supplier to the Buyer is free from all defects in material and workmanship and that components/parts/units which prove to suffer from manufacturing or any other defects will be repaired or replaced immediately free of any charge (material, labour, transit or any other incidental costs) by the Supplier within the warranty period. The Supplier also declares that the goods sold to the Buyer under this Purchase Order are of the best quality and workmanship and are strictly in accordance with the specifications. Supplier should provide Warranty Certificate duly signed and sealed to PCI along with goods.
The defects, if any, shall be attended to on immediate basis but in no case any defect should prolong for more than 24 hours. The comprehensive warranty includes onsite warranty with parts.

20). Product Support: The Seller agrees to provide product support for the PAC Article during the warranty period from the date of installation and commissioning of the materials as per our Purchase Order terms and conditions by the seller/vendor. The warranty on the associated software should cover providing of upgraded version/s, if any, released during the warranty period free of cost.
The manufacturer/OEM should facilitate the bidder/Agent on regular basis with technology / product updates & extend support for the warranty as well.

21) If as a result of post payment audit any erroneous payment payment or any over payment is made in respect of any supply/work done by the Agency it shall be recovered with prevailing interest by the NIELIT Calicut from the supplier.

22) The Bidder shall be liable to provide copies of all the relevant records during the concurrency period of Contract or otherwise even after the Contract is over, whenever required by the NIELIT, Calicut.

23).Manufacturer's name and country of origin of materials offered must be clearly specified. Any bidder from a country which shares a land border with India will be eligible to bid in this tender, only if the bidder is registered with the Competent Authority. Competent Authority for the purpose of registration shall be the Registration Committee constituted by the Department for Promotion of Industry and Internal Trade (DPIIT).

24) Public Procurement Policy:

The bidder shall be compliant to the Public Procurement (Preference to Make in India), Order 2017 as amended on 16.09.2020 (and as amended further from time to time) issued by Ministry of Finance / Department for Promotion of Industry and Internal Trade (DPIIT), Ministry of Commerce and Industry. Also bidder must submit undertaking on bidder's letterhead along with bid for local content of .... % offered in subject tender. Any false declaration and non-compliance of the above would be a ground for immediate rejection of offer or termination of the contract and further legal action in accordance with the laws.

25). Supply Agreement

The supplier is required to execute necessary agreement within two weeks upon receipt of our confirmed purchase Order.

26).Exclusive right: The Director, NIELIT Calicut, India.

The **Director, NIELIT Calicut**, Kerala, India has the full and exclusive right to accept or reject, increase or decrease order quantity, any or all the Quotation/Purchase Order without assigning any reasons thereof and also to cancel the supply order whole or any part of, at any time without assigning any reason.

<u>The OEM/Vendor shall provide the following attached documents along with the quotation.</u>

Annexure –I (General Terms and Conditions)
Annexure –II (Schedule of Requirements),
- " IIA (Detailed Specifications)
- " IIB (Compliance Sheet)
- " IIC (Specific Terms and Conditions)

Annexure –III (Price Format)
Annexure-IV (No Dues Certificate)
Annexure-V (Undertaking)
Annexure-VI (Fall Clause Certificate)
Annexure-VII (Declaration of Local Content.)

Form No. 1 : Bid Form (Covering Letter)
1.1 Bidder Information
1.2 Eligibility Declaration
1.3 Original Manufacturing Company authorisation
1.4 Declaration by Reseller/Agents/Associates of Foreign Principles

Annexure -II

Schedule of Requirements and specifications

List of FPGA Boards List and Associated Design Software Tools and Installation Services

FPGA Boards (Total of 100 nos. of Participating Institutes)			
S. No.	**FPGA Boards Name and Details**	**Quantity Per Institute**	**Total Number of Boards**
1.	Pynq Z2	6	600
2.	Pmod KYPD: 16-button Keypad	6	600
3.	Pmod OLEDrgb: 96 x 64 RGB OLED Display Pmod	6	600
4.	Pmod DA2: Two 12-bit D/A Outputs	6	600
5.	Pmod TPH2: 12-pin Test Point Header	40	4000
6.	Boolean Board	16	1600
7.	Urbana Board	2	200
8.	Arty A7-100T	1	100
9.	Kria KR-260	1	100
10.	Kria KV (Video)	1	100
11.	Pynq ZU	1	100
12.	Zynq UltraScale+ MPSoC ZCU104	1	100
13.	UEF-VIVADO-ENTER-25 (2 bundles)	1	100
14.	UEF-MATSIM-ADDON-25 (2 bundles)	1	100
15.	One-time demonstration/installation services & Technical support	1	100
FPGA Boards (Centrally Hosted/Available at C-DAC, Bengaluru)			
S. No.	**FPGA Boards Name and Details**	**Quantity Per Institute**	**Total Number of Boards**
1.	Versal VCK5000	1	1
2.	Alveo U55C	2	2
3.	UEF-VIVADO-ENTER-25 (2 bundles)	1	1
4.	UEF-MATSIM-ADDON-25 (2 bundles)	1	1
5.	One-time demonstration/installation services & Technical support	1*	1*

NB. NIEIT Calicut reserve the right to modify (increase or decrease) the quantity specified above/in this enquiry upon placing purchase order

(Letter Head) Annexure-III

PRICE FORMAT

Our Quotation No. Date:

1	Description and specification	
2	Quantity & Unit	
3	Delivery Terms	
4	Delivery Period	
5	Taxes, Duties & any other statutory levies or charges	
6	Transportation, Insurance, P & F charges, if any	
7	Discount/off etc., if any	
8	Total Rate per unit	
9	Price Value (Net Price) in Rs. (in figures & words)	
10	Warranty	

I/We engage to supply the material(s) to as per our schedule of requirements/purchase order and comply the following:

1. Tender schedule and technical specifications indicated.
2. Item/tender specific conditions for this tender
3. Terms and conditions of this Tender Enquiry/RFQ.
4. I/We confirm that set off for the ED, VAT, etc. Paid on the inputs have been taken into consideration in the above quoted price and further agree to pass on such additional duties as sets offs as may become available in future under VAT, etc.
5. This offer is valid for **90 (ninety) days** from the date of opening of the tender.
6. That we have not been debarred by the any Government/Undertaking.
7. That the rates quoted are not higher than the rates quoted for same item to any Government/Undertaking.
8. That the bid submitted by us is properly sealed and prepared so as to prevent any subsequent alteration and replacement.

Signature & Seal
Place & Date

Name of Authorised Signatory &
Address
Email id & Mobile

NB: Additional page may be added for detailed price quotation. The items with different lead times need to be specified in separate table and quoted separately.

Annexure -IV

Format for No Claim Certificate

(On company Letter-head)

Contractor's Name_____
[Address and Contact Details]
Contractor's Reference No._____ Date.....

To

The Director
National Institute of Electronics and Information Technology (NIELIT)
P.B. No. 5, NIT Campus P.O. Calicut – 673601

No Claim Certificate

Sub: Contract Agreement no. ---------- dated ----------for the supply of ----------
---

We have received the sum of Rs. (Rupees _____only) as final settlement due to us for the supply of _____under the above mentioned contract agreement.

We have received all the amounts payable to us with this payment and have no outstanding dispute of any description whatsoever regarding the amounts worked out as payable to us and received by us.

We hereby unconditionally and without any reservation whatsoever, certify that we shall have no further claim whatsoever, of any description, on any account, against the Procuring Entity, under contract above. We shall continue to be bound by the terms and conditions of the contract agreement regarding its performance.

Yours faithfully,

Signatures of contractor or
officer authorised to sign the contract documents.
on behalf of the contractor

(Company Seal)

Date:_____
Place:_____

Annexure -V

UNDERTAKING

Quotation Enquiry Ref. No. Dated:

FOR COMPLIANCE OF ALL TERMS & CONDITIONS MENTIONED IN THIS REQUEST FOR QUOTATION

(Should be printed on the Official Letter head of Manufacturer/their Authorized Distributor/Dealer)

To
The Director,
NIELIT CALICUT,
P.O. NIT CAMPUS, CALICUT – 673601,
KERALA

Sir,

1. The undersigned certify that I/we have gone through the terms and conditions mentioned in the tender enquiry Document and undertake to comply with them. I have no objection for any of the content of the tender enquiry Document and I undertake not to submit any complaint/ representation against the tender enquiry Document after submission date and time of the tender documents. The rates quoted by me/us are valid and binding on me/us for acceptance till the validity of tender.

2. I/We undersigned hereby bind myself/ourselves to National institute of Electronics and Information Technology (NIELIT) Calicut, Kerala, India to supply the approved awarded Article/Software on receipt of approved Purchase Order.

3. The Proprietary articles shall be of the best quality and of the kind as per the requirement of the institution. The decision of the Executive Director, NIELIT Calicut, India (herein after called the said officer) as regard to the quality and kind of article shall be final and binding on me.

4. In case our quotation is accepted and order is placed, the supply against the order will be made within the period stipulated in the purchase order.

5. If I/We fail to supply the stores in stipulated period the NIEIT Calicut has full power to impose LD and deduct the applicable amount from our pending Bills and take appropriate action deemed fit against our firm.

6. I/We declare that no legal/financial irregularities are pending against the proprietor/partner of the participating firm or manufacturer.

7. If any purchase order placed by NIELIT, Calicut, I/we undertake to supply the order within the stipulated period and if fail to supply order during the stipulated period the necessary action can be taken by the Director, NIELIT Calicut, India against our firm.

8. I/We undertake that if the rates of any items are lowered due to any reason, I will charge the lower rates.

9. I/We undertake that the quoted rates are not higher than that approved in any other Govt. institutions in India for the same items during the current Financial Year.

10. No CBI Inquiry/FEMA/Criminal proceeding/Black listing is pending or going on against the manufacturer/bidder firm. I/We undertake that I will not submit any irrelevant documents with the offer and if any time it is found that I have done any such mistake, I will not have any objection if my Proposal is rejected on that ground.

11. I/We undertake that any issues related with Proprietary Article/Intellectual Proprietary Rights shall solely be taken care by us and we shall be responsible for any kind of issue that arise during concurrency of supply order and we also undertake that; we shall indemnify, NIELIT Calicut in all such related matters.

12. I/We undertake to supply the all Literature (Catalog/Log Book/Maintenance Record/Troubleshooting/Operation Manuals etc.) supplied with each of item provided by Principal Manufacturer in Original to (if any applicable).

13. I/We do hereby confirm that the prices/rates quoted are fixed and are at par with the prices quoted by me/us to any other Govt. of India/ Organisation/Academic Institutions/PSUs. I/we also offer to supply the Equipment/stores/goods/items at the prices and rates not exceeding those mentioned in our Price Quotation offer.

14. I/we undertake, If as a result of post payment audit any over payment is made in respect of any Supply/work done by our Agency or alleged to have been done by our Agency under this tender enquiry it shall be recovered by the NIELIT Calicut from our Agency.

15. I/we undertake that we shall liable to provide all the relevant records copies during the concurrency period of Contract or otherwise even after the Contract is over, whenever required by NIELIT Calicut

16. I/We undertake that we shall deposit Performance Security of 3% value of Supply Orders issued to us by NIELIT Calicut in favor of "Executive Director, NIELIT Calicut" in the form of FDR/Performance Security Bank Guarantee from Scheduled Bank in India for entire warranty period plus 60 days. If we fail to fulfill the Contractual obligation/any breach of Contract/not honor Purchase Order of NIELIT Calicut during Rate Contract Period, the NIELIT Calicut should have full right to forfeiture of our Performance Security Deposit Amount in total.

Affirmation

I pledge and solemnly affirm that the information submitted in tender/quotation documents is true to the best of my knowledge and belief. I further pledge and solemnly affirm that nothing has been concealed by me and if anything adverse comes to the notice of purchaser during the validity of Purchase order/Contract period. The Executive Director, National Institute of Electronics and Information Technology (NIELIT Calicut) will have full authority to take appropriate action deemed fit against our firm.

Signature of Bidder
(Name of Bidder)

Place .....
Date.....

With seal of firm

(Letter head) Annexure - VI

FALL CLAUSE NOTICE CERTIFICATE

This is to certify that we have offered the maximum possible discount to you in our Quotation No. _____ dated _____

The prices charged for the Stores supplied under tender should under no event be higher than the lowest prices at which the party sells the items of identical description to any other Govt. organization/PSU's/Central Govt, /State Govt. Autonomous bodies/Central/state Universities/Central/State Educational Institutions, failing which the "FALL CLAUSE" will be applicable. The institute will look into a reasonable past period to ensure this.

In case, if the price charged by our firm is found to be more, NIELIT Calicut will have the right to recover the excess charged amount from the subsequent/unpaid bill of the supplier.

Note: This letter of authority should be on the letterhead of the quoting firm and should be signed by a Competent Authority and having the power of attorney

Annexure-VII

Declaration for Local Content on OEMs Letter Head

(To be given on Company Letter Head - For tender value below Rs.10 Crores) (To be given by Statutory Auditor/Cost Auditor/Cost Accountant/CA for tender value above Rs.10 Crores)

Date: _____

To,

The Director,

National institute of Electronic and Information Technology (NIELIT)

P.B. No. 05, NIT Campus

Calicut – 673 601, Kerala

Sub: Declaration of Local content

Tender Reference No: No16(70)/2023/C2S/FPGA

Name of Tender / Work: -

_____ 1.

Country of Origin of Goods being offered: _____

2. We hereby declare that items offered has ____% local content **(Please provide exact %).**

3. Details of location at which local value addition will be made / made: (Complete address to be mentioned) _____

_____

"Local Content" means the amount of value added in India which shall, be the total value of the item being offered minus the value of the imported content in the item (including all customs duties) as a proportion of the total value, in percent.

"*False declaration will be in breach of Code of Integrity under Rule 175(1)(i)(h) of the General Financial Rules for which a bidder or its successors can be debarred for up to two years as per Rule 151 (iii) of the General Financial Rules along with such other actions as may be permissible under law."

Yours Faithfully,

(Signature of the Bidder/OEM, with Official Seal)

Bid Form (Covering Letter)

(On Bidder's Letter-head)

(Strike out alternative phrases not relevant to you)

Bidder's Name_____
[Address and Contact Details]

Bidder's Reference No._____ Date…….

To
The Director
NIELIT CALICUT
P.B. No.05. P.O. NIT Campus
CALICUT- 673601, Kerala

Ref: Your Tender Document No.**16(70)/2023/C2S/FPGA** Tender Title **: Supply of FPGA Boards and Associated Design Software Tools and Installation Services**: Reg.

Sir/ Madam

Having examined the above mentioned Tender Document, we, the undersigned, hereby submit our Quotation/Price Schedule for the supply of **FPGA Boards and Associated Design Software Tools and Installation Services** is in conformity with the said Tender Documents.

(Please tick appropriate boxes or strike out sentences/ phrases not applicable to you)

1) **Our Credentials:**

(a) We are submitting this bid: -

- □ on our behalf, and there are no agents/ dealers involved in this tender, and hence no agency agreement or payments/ commissions/ gratuity is involved. Our company law and taxation regulatory requirements and authorization for signatories and related documents are submitted in Form 1.1 (Bidder Information).

Or

- □ as authorised dealer offering goods manufactured by our OEMs. Our OEM's law and taxation regulatory requirements and authorization for signatories and related documents are submitted in Form 1.3 (OEM's Authorization).

Or

- □ as agents/associates of our foreign principals. Our foreign principal's law and taxation regulatory requirements, as well as authorization for signatories and related documents, are submitted in Form1.4 (Declaration by Agents/ Associates of Foreign Principals/ OEMs).

(a) We…….. hereby certify that □ We/ □ our Principals/ OEM M/ s……. are proven, established, and reputed manufacturers with factories at …… which are fitted with modern equipment and where the production methods, quality control, and testing of all materials and parts manufactured or used by us shall be open to inspection by the representative of the Procuring Entity.

2) **Our Eligibility and Qualifications to participate**

We comply with all the eligibility criteria stipulated in this Tender Document, and the relevant declarations are made along with documents in Form 1.2 of this bid-form.

3) **Our Bid to supply Goods:**

We offer to supply the subject Goods of requisite quality and within Delivery Schedules in conformity with the Tender Document.

4) **Prices:**

We hereby offer to perform the Services at our lowest prices and rates mentioned in the separate Price-Schedule. It is hereby confirmed that the prices quoted therein by us are:

(a) based on terms of delivery.

(b) Cost break-up of the quoted cost, showing inter-alia costs (including taxes and duties thereon) of all the included incidental Goods/ Works considered necessary to make the proposal self-contained and complete, has been indicated therein, and

(c) based on the terms and mode of payment as stipulated in the Tender Document.

5) **Affirmation to terms and conditions of the Tender Document:**

We have understood the complete terms and conditions of the Tender Document. We accept and comply with these terms and conditions without any reservations.

6) **Bid Securing Declaration**

We have submitted the Undertaking for EMD/Bid Security Declaration, in lieu of Bid Security in stipulated format vide Annexure -IV.

7) **Abiding by the Bid Validity**

We agree to keep our bid valid for acceptance for a period upto ……, as required in the Tender Document or for a subsequently extended period, if any, agreed to by us and are aware of penalties in this regard stipulated in the Tender Document in case we fail to do so.

8) **Non-tampering of Tender Document and document Copies**

We confirm that we have not changed/ edited the contents of the Tender Document. We realise that any such change noticed at any stage, including after the contract award, shall be liable to punitive action in this regard stipulated in the Tender Document. We also confirm that scanned copies of documents/ affidavits/ undertakings submitted along with our quotation/bid/offer are valid, true, and correct to the best of our knowledge and belief. If any dispute arises related to the validity and truthfulness of such documents/ affidavits/ undertakings, we shall be responsible for the same. Upon accepting our offer/quotation/bid, we undertake to submit for scrutiny, on-demand by the NIELIT Calicut, originals, and self-certified copies of all such certificates, documents, affidavits/ undertakings.

9) **A Binding Contract:**

We further confirm that, if our bid is accepted, all such terms and conditions shall continue to be acceptable and applicable to the resultant contract, even though some of these documents may not be included in the contract Documents submitted by us. We do hereby undertake that, until a formal contract is signed or issued, this bid, together with your written Letter of Award (LoA)/Purchase Order shall constitute a binding contract between us.

10) **Performance Guarantee**

We further confirm that, if our bid is accepted, we shall provide you with performance security of the required amount stipulated in the Tender Document for the due performance of the contract. We are fully aware that in the event of our failure to deposit the required security amount, the NIELIT Calicut has the right to avail any or all punitive actions laid down in this regard, stipulated in the Tender Document.

11) **Signatories:**

We confirm that we are duly authorized to submit this bid and make commitments on behalf of the Bidder. Supporting documents are submitted in annexed herewith.

12) **Rights of the Procuring Entity to Reject bid(s):**

We further understand that you are not bound to accept our offer as against your above-referred Tender Document.

……..
(Signature with date)
……..
(Name and designation)
Duly authorized to sign bid for and on behalf of
[name & address of Bidder and seal of company]

Form No.1.1

Bidder Information

(On Company Letter-head)
(Along with supporting documents, if any)

Bidder's Name_____
[Address and Contact Details]

Bidder's Reference No._____ Date…….

Tender Document. **No. 16(70)/2023/C2S/FPGA** Tender Title: **Supply of FPGA Boards and Associated Design Software Tools and Installation Services : Reg**

Note: Bidder shall fill in this Form following the instructions indicated below. No alterations to its format shall be permitted, and no substitutions shall be accepted. Bidder shall enclose certified copies of the documentary proof/ evidence to substantiate the corresponding statement wherever necessary and applicable. Bidder's wrong or misleading information shall be treated as a violation of the Code of Integrity. Such Bids shall be liable to be rejected as nonresponsive, in addition to other punitive actions provided for such misdemeanours in the Tender Document.

(Please tick appropriate boxes or strike out sentences/ phrases not applicable to you)

1) **Bidder/ Contractor particulars:**

(a) Name of the Company:…….
(a) Corporate Identity No. (CIN): ……..
(b) Registration, if any, with The Procuring Entity: ……..
(c) Place of Registration/ Principal place of business/ manufacture …….
(d) Complete Postal Address: ……..
(e) Pin code/ ZIP code: …….
(f) Telephone nos. (with country/ area codes): ……
(g) Mobile Nos.: (with country/ area codes): ……..
(h) Contact persons/ Designation: …….
(i) Email IDs: …….

Submit documents to demonstrate eligibility. A self-certified copy of registration certificate – in case of a partnership firm – Deed of Partnership; in case of Company – Notarized and certified copy of its Registration; and in case of Society – its Byelaws and registration certificate of the firm.

2) **Taxation Registrations:**

(a) PAN number: ……..
(j) Type of GST Registration as per the Act (Normal Taxpayer, Composition, Casual Taxable Person, SEZ, etc.): …….
(k) GSTIN number: ……. in Consignor and Consignee States
(l) Registered/ Certified Works/ Factory where the Goods would be mainly manufactured and Place of Consignor for GST Purpose: …….
(m) Contact Names, Nos. & email IDs for GST matters (Please mention primary and secondary contacts): ……

☐ We solemnly declare that our GST rating on the GST portal/ Govt. official website is not negative/ blacklisted.

Documents to be submitted: Self-attested Copies of PAN card and GSTIN Registration.

3) **Authorization of Person(s) signing the bid on behalf of the Bidder**

(a) Full Name: _____
(n) Designation: _____
(o) Signing as:

- A sole proprietorship firm. The person signing the bid is the sole proprietor/ constituted attorney of the sole proprietor,
- A partnership firm. The person signing the bid is duly authorised being a partner to do so, under the partnership agreement or the general power of attorney,
- A company. The person signing the bid is the constituted attorney by a resolution passed by the Board of Directors or in pursuance of the Authority conferred by Memorandum of Association.

Documents to be submitted: Registration Certificate/ Memorandum of Association/ Partnership Agreement/ Power of Attorney/ Board Resolution.

4) **Bidder's Authorized Representative Information**

(a) Name:
(p) Address:
(q) Telephone/ Mobile numbers:
(r) Email Address:

(Signature with date)
……..
(Name and designation)
Duly authorized to sign bid for and on behalf of
[name & address of Bidder and seal of company]
DA: As above
…….

Eligibility Declarations

(On Company Letter-head)

(Along with supporting documents, if any)

Tender Document No.16(70)/2023/C2S/FPGA
Tender Title**: Supply of FPGA Boards and Associated Design Software Tools and Installation Services: Reg**

Bidder's Name_____
[Address and Contact Details]
Bidder's Reference No._____ Date…….

Note: The list below is indicative only. You may attach more documents as required to confirm your eligibility criteria.

Eligibility Declarations

(Please tick appropriate boxes or cross out any declaration not applicable to the Bidder)

We hereby confirm that we comply with all the stipulation of Request for Quotation/Tender and declare as under and shall provide evidence of our continued eligibility to the Procuring Entity as may be requested:

1) **Legal Entity of Bidder:** _____

1) **OEM/ Manufacturer/ Agent/ Dealership Status:** _____

2) We □ are/ □ are not a JV_____

3) We solemnly declare that we (including our affiliates or subsidiaries or constituents):

   a) are not insolvent, in receivership, bankrupt or being wound up, not have our affairs administered by a court or a judicial officer, not have our business activities suspended and are not the subject of legal proceedings for any of these reasons;
   b) (including our Contractors/ subcontractors for any part of the contract):
      (i) Do not stand declared ineligible/ blacklisted/ banned/ debarred by the NIELIT or its Ministry/ Department from participation in its Tender Processes; and/ or
      (ii) Are not convicted (within three years preceding the last date of bid submission) or stand declared ineligible/ suspended/ blacklisted/ banned/ debarred by appropriate agencies of Government of India from participation in Tender Processes of all of its entities, for offences mentioned in Tender Document in this regard. We have neither changed our name nor created a new "Allied Firm", consequent to the above disqualifications.
   c) Do not have any association (as bidder/ partner/ Director/ employee in any capacity) with such retired public official or near relations of such officials of Procuring Entity, as counter-indicated, in the Tender Document.
   d) We certify that we fulfill any other additional eligibility condition if prescribed in Tender Document.
   e) We have no conflict of interest, which substantially affects fair competition. The prices quoted are competitive and without adopting any unfair/ unethical/ anti-competitive means. No attempt has been made or shall be made by us to induce any other bidder to submit or not to submit an offer to restrict competition.

4) **Restrictions on procurement from bidders from a country or countries, or a class of countries under Rule 144 (xi) of the General Financial Rules 2017:**
   We certify as under:

   "We have read the clause regarding restrictions on procurement from a bidder of a country which shares a land border with India and on sub-contracting to contractors from such countries, and solemnly certify that we fulfil all requirements in this regard and are eligible to be considered. We certify that:

(a) *we are not from such a country or, if from such a country, we are registered with the Competent Authority (copy enclosed). and;*

(b) *we shall not subcontract any work to a contractor from such countries unless such contractor is registered with the Competent Authority.*

5) **MSME Status:**

Having read and understood the Public Procurement Policy for Micro and Small Enterprises (MSEs) Order, 2012 (as amended and revised till date), and solemnly declare the following:

a) We are - Micro/ Small/ Medium Enterprise/ SSI/ Govt. Deptt. / PSU/ Others:……

b) We attach herewith, Udhyam Registration Certificate with the Udhyam Registration Number as proof of our being MSE registered on the Udhyam Registration Portal. The certificate is the latest up to the deadline for submission of the bid.

c) Whether Proprietor/ Partner belongs to SC/ ST or Women category. (Please specify names and percentage of shares held by SC/ ST Partners):…….

6) **Start-up Status**

We confirm that we □ are/ □ are not a Start-up entity as per the definition of the Department of Promotion of Industrial and Internal Trade – DPIIT.

We also declare that

□ There is no country whose bidders have been notified as ineligible on a reciprocal basis under this order for the offered Goods, or

□ We do not belong to any Country whose bidders are notified as ineligible on a reciprocal basis under this order for the offered Goods.

7) **Self-Declaration by Indian Agents/ Associates of Foreign Principals**

(a) Self-attested documentary evidence about their identity (PAN, Aadhar Card, GSTIN registration, proof of address, etc.), business details (ownership pattern and documents, type of firm, year of establishment, sister concerns etc.) to establish that they are a bonafide business as per Indian Laws – are submitted as part of Form 1.1 annexed herewith.

(b) Agency Agreement shall be submitted with Form 1.4. It shall cover

(i) the precise relationship, services to be rendered, mutual interests in business - generally and/ or specifically for the tender and

(ii) any payment the agent or associate receives in India or abroad from the foreign OEM/ principal, whether a commission or a general retainer fee.

(c) Our Foreign principals, explicitly authorizing us to make an offer in response to the tender, either directly or in association with them, are listed in Form 1.3 and 1.4 annexed herewith. That also indicates their name, address, nationality, status (i.e., whether manufacturer or agents of manufacturer holding the Letter of Authority of the Principal).

8) **Penalties for false or misleading declarations:**

We hereby confirm that the particulars given above are factually correct and nothing is concealed and undertake to advise any future changes to the above details. We understand that any wrong or misleading self-declaration would violate the Code of Integrity and attract penalties as mentioned in this Tender Document.

……..
(Signature with date)
……..
(Name and designation)
Duly authorized to sign bid for and on behalf of
…….
…….
[name & address of Bidder and seal of company]

Form No. 1.4

Declaration by Agents/ Associates of Foreign Principals

(On Company Letter Head -Along with supporting documents, if any)

Agent's Name_____
[Address and Contact Details]

Principal's Reference No._____ Date…….

The Executive Director
NIELIT Calicut
PB. No. 05, NIT Campus P.O
CALICUT – 673601, Kerala State

Dear Sirs,

Ref. Your Tender RFQ No.16(70)/2023/C2S/FPGA Tender Title**: Supply of FPGA Boards and Associated Design Software Tools and Installation Services : Reg**.

1) We, ……., are a bonafide business as per Indian Laws. We have been retained as agent/ associates by our foreign principals/ OEM, Messrs…….. (*name and address of the principal*) to associate with them for participation in this Tender Process.

1) We understand that any failure or non-disclosures, or mis-declarations by us, shall be treated as a violation of the Code of Integrity. Our Bids shall be liable to be rejected as nonresponsive, in addition to other punitive actions by the Procuring Entity as per the Tender Document.

2) The required details are given below:.

(a) Name of the Agent/ Associate:…….
(a) Documents regarding ownership pattern: as appropriate – Bye Laws/ Registration Certificate/ Memorandum of Association/ Partnership Agreement/ Power of Attorney/ Board Resolution.
(b) Year of establishment……..
(c) Sister Concerns……..,
(d) Corporate Identity No. (CIN): ……..
(e) Aadhar Card of Owner/ CEO/ Partner
(f) PAN number: ……
(g) Complete Postal Address: ……..
(h) Pin code/ ZIP code: …….
(i) Telephone nos. (with country/ area codes): ……
(j) Mobile Nos.: (with country/ area codes): ……..
(k) Contact persons/ Designation: …….
(l) Email IDs: …….
(m) Type of GST Registration (Registered, Unregistered, Composition, SEZ, RCM etc.): …….
(n) GSTIN number: ……. in Consignor and Consignee States

(o) Registered office from where agency/ association services would be mainly provided for GST Purpose: …….

(p) Contact Names, Nos. & email IDs for GST matters (Please mention primary and secondary contacts): ……

3) Details required regarding the foreign principal/ OEM are given below.

(a) Name of the Company:…….

(q) Nationality/ Country of operation/ incorporation……

(r) Status:

(i) manufacturer or

(ii) agents of manufacturer holding the Letter of Authority of the Principal, specifically authorizing the agent to make an offer in India in response to tender either directly or through the agents/ representatives.

(s) Complete Postal Address: ……..

(t) Telephone nos. (with country/ area codes): ……

(u) Mobile Nos.: (with country/ area codes): ……..

(v) Contact persons/ Designation: …….

(w) Email IDs: …….

4) We enclose herewith: as appropriate, our ---------- Bye-Laws/ Registration Certificate/ Memorandum of Association/ Partnership Agreement/ Power of Attorney/ Board Resolution

Yours faithfully,

……..……..

……

[signature with date, name, and designation]

for and on behalf of Messrs……

[name & address of the OEM and seal of company]