राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान (रा.इ.सू.प्रौ.सं.), कालिकट

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT), CALICUT

(An Autonomous Scientific Society of Ministry of Electronics & Information Technology, Government of India)

NIT Campus PO, CALICUT - 673 601

0495 2287266; Web: http://nielit.gov.in/calicut

National Institute of Electronics and Information Technology (NIELIT) Calicut is a premier organization engaged in Education, Training, R&D and Consultancy in the areas of Electronics, IT and ITES. We conduct courses both in the formal (M.Techs) and Non-formal (PG Diplomas and customized courses etc.) sectors. We require the following personnel on contract basis.

PROJECT ENGINEER – TOTAL - 3 POSTS

Project	**Special Manpower Development Program – Chip to System Design (SMDP-C2SD)**
No. Of Posts	**01**
Qualification:	Essential : BE/B.Tech in Electronics and Communication/Bio-Medical Engineering/Medical Electronics/Electronics and Instrumentation/Computer Science and allied branches/MSc in Electronics/Computer Science.
Requirement	Knowledge in Verilog, C/C++, Knowledge in System Verilog and UVM will be an added advantage.
Preferred Skills	Knowledge in CADENCE EDA Tools for Digital, Analog Mixed Signal VLSI, RTL 2 GDSII Design Flow and Analog Circuits Design.
Age	Up to 35 Years
Selection Process	Candidates will be selected based on their performance in test/interview.
Duration of engagement	6 months or upto the duration of the project whichever is earlier
Remuneration	₹18000/- to ₹25000/- per month (consolidated) based on qualification, experience and performance in the Interview.

WALK-IN-INTERVIEW

Date : **12.01.2018**
Time: **9.00 AM**
Venue : **NIELIT, Calicut**

Project	**Indigenous Color Doppler Ultrasound Scanner with PNDT Compliance (ICDU)**
No. Of Posts	**02**
Qualification:	Essential : BE/B.Tech in Electronics and Communication/Bio-Medical Engineering/Medical Electronics/Electronics and Instrumentation/Computer Science and allied branches/MSc in Electronics/Computer Science.
Desirable	ME/M.Tech in Computer Science/Embedded Systems
Requirement (Software)	RTOS porting and application software development, Driver bring up and GUI development in QT platform, System Integration and Testing. Domain knowledge in Digital Signal and Image Processing
Requirement (Hardware)	Knowledge of ORCAD EDA Tool. Exposure to High Speed Digital Design, Verilog RTL Coding, PCIe Protocol knowledge. Domain knowledge in Digital Signal and Image Processing
Preferred Skills	(**Software**) Experience in Device Driver Development, GUI Development in QT and C/C++ (**Hardware**) Experience in High Speed Digital Design, Board Design Flow
Age	Up to 35 Years
Selection Process	Candidates will be selected based on their performance in test/interview.
Duration of engagement	6 months or upto the duration of the project whichever is earlier
Remuneration	₹18000/- to ₹25000/- per month (consolidated) based on qualification, experience and performance in the Interview.

WALK-IN-INTERVIEW

Date : **12.01.2018**
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LAB ENGINEER – 1 POST

Project	**Special Manpower Development Program – Chip to System Design (SMDP-C2SD)**
No. Of Posts	**010.**
Qualification:	Essential : BE/B.Tech in Electronics and Communication/Bio-Medical Engineering/Medical Electronics/Electronics and Instrumentation/Computer Science and allied branches/MSc in Electronics/Computer Science.
Desirable	ME/M.Tech in VLSI Design/VLSI and Embedded Systems/Electronic Design Technology
Requirement	Knowledge in Verilog, C/C++, Knowledge in System Verilog and UVM will be an added advantage.
Preferable	Experience in ASIC Verification using SV and UVM
Age	Up to 35 Years
Selection Process	Candidates will be selected based on their performance in test/interview.
Duration of engagement	6 months or upto the duration of the project whichever is earlier
Remuneration	₹18000/- to ₹25000/- per month (consolidated) based on qualification, experience and performance in the Interview.

Interested candidates may appear for a Walk-in-Interview at our Institute on **12.01.2018** at **09.00 AM sharp.**

Candidates should bring with them all **original documents** in support of their age, qualifications, experience, Identity and address proof etc. along with a copy of signed Bio-data. The candidates will not be eligible for any TA for attending test/interview. Candidates who have the relevant qualification required for the above post **only** need to appear for the selection.

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WALK-IN-INTERVIEW

Date : **12.01.2018**
Time : **9.00 AM**
Venue : **NIELIT, Calicut**