राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान ,कालीकट
National Institute of Electronics & Information Technology, Calicut
(An Autonomous Scientific Society of Ministry of Electronics & Information Technology, Government of India)
NIT Campus PO, CALICUT - 673 601
✆ 0495 2287266; Web: http://nielit.gov.in/calicut

RECRUITMENT NOTIFICATION No. *3(133)/97/Dec 21/01*

Last date for submitting the application is 31 Dec 2021

National Institute of Electronics and Information Technology (NIELIT) Calicut is a premier organization engaged in Education, Training, R&D and Consultancy in the areas of Electronics, IT and ITES. We conduct courses both in the formal (M. Tech) and Non-formal (PG Diplomas and customized courses etc.) sectors. We also conduct online proctored examination and Recruitment Activity.

National Institute of Electronics & Information Technology (NIELIT) Calicut, invites applications for Project Associate posts purely on contract basis for the project:

***"Design and Implementation of digital beam forming algorithms on FPGA, Multi-Core and GPU platforms and investigation of performance matrices",* funded by Defence Research and Development Organization (DRDO), Naval Research Board (NRB).**

Details	Project Associate II (VLSI/ES)	Project Associate I (VLSI)	Project Associate I (ES)
Number of Posts	1	1	1
Consolidated Salary per month	**Rs.37,800/-**	**Rs.33,480/-**	**Rs.33,480/-**
Qualification Essential	M.E/M.Tech. in VLSI Design/Embedded systems/Electronic Design Technology/Signal processing/Communication systems or PG Diploma in VLSI/Embedded systems.	B.E/ B.Tech in Electronics/ ECE/EEE/CSE and allied branches.	B.E/ B.Tech in Electronics/ ECE/EEE/CSE and allied branches.
Desirable Qualification	1-2 Years of experience in VLSI/FPGA domain	M.E/M.Tech. in VLSI Design/Electronic Design Technology etc. or PG Diploma in VLSI Design.	M.E/M.Tech. in Computer Science/ Embedded Systems, etc. or PG Diploma in Embedded systems.
Age Limit	Below 40 Years	Below 35 Years	Below 35 Years
Desirable Domain : Knowledge & Experience	**VLSI & FPGA Domain**: FPGA implementation of Signal processing Algorithms. Knowledge in digital beam forming techniques. Good knowledge in Verilog HDL coding.	**VLSI & FPGA Domain**: Knowledge in FPGA/ASIC design flow. Good knowledge in Verilog HDL coding.	**Embedded Systems Domain:** Knowledge of Embedded Linux/RTLinux, RTLinux porting, Signal processing Algorithms implementation on Multi-Core SoC/GPU, Testing, Debugging, bench marking, profiling knowledge, Optimization and knowledge of using standard libraries like Intel IPP, Customization of Linux /RTLinux Kernel, Knowledge of Embedded Hardware architectures.

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Details	Project Associate II (VLSI/ES)	Project Associate I (VLSI)	Project Associate I (ES)
Job Description/ Profile	VLSI architecture Development and FPGA implementation of complex signal processing algorithms. Good knowledge in digital beam forming techniques in RADAR/SONAR/Medical Ultrasound systems. Verilog HDL coding, FPGA Design Flow.	FPGA implementation of signal processing algorithms, Verilog HDL Coding, and RTL verification. Debugging using embedded logic analyzer.	Implementation of Signal processing Algorithms on Multi-Core SoC/GPU, testing, debugging, bench marking, profiling and optimization. Customization of Linux /RTLinux Kernel for Embedded Hardware architectures.
Duration of Engagement	Initially for 6 Months. Extendable up to the entire duration of the project.		
Selection Process:	Screened-in candidates will be selected based on their performance in test/Interview.		

General Instructions

- Application should be submitted only online through Link: https://forms.gle/LiARYzfNSbjTvcpN6
- Only Indian nationals are eligible to apply.
- Canvassing in any form will be a disqualification.
- No interim enquiry / correspondence, whatsoever, will be entertained regarding the recruitment.
- Incomplete applications are liable to be summarily rejected.
- NIELIT Centre Calicut reserves the right to fill or not to fill the post(s) advertised.
- There will be no application fee required to be paid.
- Candidates with relevant experience will be preferred. However, the same may be relaxed in deserving cases.
- The vacancies notified are tentative and are subject to change.
- Experience is counted only for the period after obtaining the eligibility qualification.
- Applications, which are not in conformity with the requirements indicated are liable to be rejected.
- The Institute will have the right to fix criteria for screening the applications so as to reduce the number of candidates to be called for interview.
- Only short-listed candidates will be called for Written Test/interview. Mere fulfilling of requirements as laid down in the advertisement does not qualify a candidate for interview.
- No TA/DA will be provided to attend the interview.
- Applicant should have a valid/Active G-mail account for submitting application.
- Hostel facility will be provided to selected candidates on payment basis as per availability.
- Candidate will be rejected, if the information provided by the candidate is found incorrect/failed to produce documentary proof on qualification etc.
- It is the responsibility of the candidate to obtain NOC etc from the current employer/institution, in case already bound by any contract.