

National Institute of Electronics & Information Technology, Haridwar

(Ministry of Electronics & Information Technology, Government of India)

VLSI Design using Verilog

Course Objective

This course is intended to impart training in designing and verifying reusable Intellectual Property (IP) Cores for VLSI. Emphasis of the teaching curriculum is on design & Verification methodologies and on its practical applications. The course contents have been designed keeping in view the emerging trends in needs for skilled manpower.

Eligibility

B.E/B.Tech/MCA/M.Sc.(Comp.Sc.) (pursuing also) with basic knowledge of statistics, database and any programming language.

Course Outline

- Overview of VLSI, Verilog and Digital Design.
- Hierarchical Modelling
- Modules and Ports definition
- Gate Level Modelling
- Data Flow modelling
- Behavioural Modelling
- Structural Modelling

e-Certificate

e-Certificate will be issued to each participant after the completion of the training. Participant needs to maintain minimum 75% attendance during the online classes and is required to score minimum 50% marks in the online test in order to successfully complete the course.

Course Duration

04 weeks

Prerequisites for Online Class

Candidate must have ModelSim software installed and latest computer/laptop with preferably 4 GB RAM or higher.

How to Apply ?

Candidate may apply online at following link: <http://nielit.gov.in/haridwar/content/online-courses>. Fee is to be submitted to the following account and details to be submitted in online registration form.

Name	NIELIT Haridwar
Account No.	12922122001331
IFSC No.	PUNB0129210
Bank Name	Punjab National Bank
Branch	SIDCUL Haridwar

For Registration



For any further information/clarification, please contact on **936849990**.

Contact Details: NIELIT Haridwar, 2nd Floor, Government Polytechnic Building, Plot No-6C, Sector-11, Near Pentagon Mall, SIDCUL, Haridwar, Uttarakhand – 249403, **Phone:-** 01334-235617, 235054, 9368349990 **E-Mail:** haridwar@nielit.gov.in