No. of Printed Pages : **3**

Sl. No.

C0-R4.B4 : COMPUTER SYSTEM ARCHITECTURE

NOTE :

1. Answer question 1 and any FOUR questions from 2 to 7.

2. Part of the same question should be answered together and in the same sequence.

Total Time : 3 Hours **Total Marks : 100**

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1. (a) What is fixed point representation ? Represent (−43.625) in fixed point (assume the numbers uses 32 bit format).

(b) The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each block. Formulate the logical and physical address formats.

(c) Why are the read and write control lines in a DMA controller bidirectional ? Under what condition and for what purpose are they used as inputs and as outputs ?

(d) What are the steps involved in instruction cycle ? Explain with an example.

(e) Distinguish between multicomputers and multiprocessors based on their inter-processor communications.

(f) An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right ? Starting from the initial number 10011 100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

(g) Briefly explain the two different types used in MIMD by which multiple memory is linked via Interconnection Network. **(7x4)**

2. (a) Explain (in brief) different types of cache mapping used in the computer architecture.

(b) The following program is stored in the memory unit of the basic computer. Show the contents of the AC and PC (in hexadecimal) at the end, after each instruction is executed. All numbers listed below are in hexadecimal.

Location	Instruction
010	CLA
011	ADD 016
012	BUN 014
013	HLT
014	AND 017
015	BUN 013
016	C1A5
017	93C6

(c) Write an assembly language program, that clears the contents of hexadecimal locations 500 through 5FF to 0. **(6+6+6)**

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3. (a) What are the structural hazards and data dependencies in pipelining ?

(b) Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate the following :

(i) Pipeline cycle time

(ii) Non-pipeline execution time

(iii) Speed up ratio

(iv) Pipeline time for 1000 tasks

(v) Sequential time for 1000 tasks

(vi) Throughput

(c) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. **(6+6+6)**

4. (a) A computer employs RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(i) How many RAM and ROM chips are needed ?

(ii) Draw a memory-address map for the system.

(iii) Give the address range in hexadecimal for RAM, ROM, and interface.

(b) A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries :

Page	Block
0	3
1	1
4	1
6	0

Make a list of all virtual addresses (In decimal) that will cause a page fault if used by the CPU.

(c) What is direct memory access ? Describe DMA transfer in a computer system in which a DMA controller transfers 16 bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer ? **(6+6+6)**

5. (a) How many characters per second can be transmitted over a 1200-baud line in each of the following modes ? (Assume a character code of eight bits.)

(i) Synchronous serial transmission.

(ii) Asynchronous serial transmission with two stop bits.

(iii) Asynchronous serial transmission with one stop bit.

(b) Design a parallel priority interrupt hardware for a system with four interrupt sources.

(c) What is Booth algorithm for multiplication ? Draw a flowchart for booth algorithm. **(6+6+6)**

6. (a) What is reduced instructions set computer ? What are the differences between RISC and CISC ?

(b) What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for such type of instruction to bring an operand into a processor register ?

(c) (i) The following transfer statements specify a memory. Explain the memory operation in each case.

a. R2 <-- M[AR] b. M[AR} <-- R3 c. R5 <-- M[R5]

(ii) Represent the following conditional control statements by two register transfer statements with control functions.

If (A = 0) then (R1 <-- R2)

else If (B = 0) then (R1 <-- R3) **(6+6+6)**

7. (a) Define the Flynn's classification of various computer architectures.

(b) Explain Centralized shared memory architectures with block diagram and list out its advantages and disadvantages.

(c) Explain Distributed shared memory architectures with block diagram, specify its type and list out its advantages and disadvantages. **(6+6+6)**

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