C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is the significance of 2's compliment and 10's compliment in computer architecture? Write 10's complements of 673.
b) What are the limitations of programmed I/O?
c) Differentiate between RICS and CISC architectures.
d) Differentiate between pipelined and non pipelined computers.
e) Differentiate between direct memory and associate memory mapping.
f) Differentiate between SISD and MIMD architectures.
g) Define
   i) Tri-state devices
   ii) Instruction decoding

(7x4)

2.

a) Explain the basic Vow-Neumann Machine cycle. How timing and control is provided by hardwired control unit for ADD and SUB operation.
b) Discuss different addressing modes used in computer systems? Explain them with the help of suitable example.

(9+9)

3.

a) A 16 bit register is a computer system consists of value 1110111011000001. What will be the 10 register value when following operations are executed?
   i) arithmetic shift left
   ii) arithmetic shift right
   iii) logical shift left
   iv) logical shift right
   v) circular shift
b) What is DMA? Draw the block diagram and explain it in detail.

(10+8)

4.

a) What are the advantages of byte addressing over word addressing and what are their disadvantages?
b) What is the difference between access time and cycle time of a memory? Which is larger?
c) Define assembly language? State its advantages over higher level language.

(6+6+6)

5. The access time of a cache memory is 50ns and that of the main memory is 500ns. It is estimated that 80% of the main memory requests are for read operation and the remaining are for write. The hit ratio for read access only is 0.9 and a write through policy is used. (i) What is the average access time of the system considering only memory read cycles? (ii) What is the average access time of the system for both read and write requests? (iii) What is the hit ratio taking into consideration the write cycle?

(18)

6.

a) The 8-bit registers A, B, C & D are loaded with the value $(F2)_H$, $(FF)_H$, $(B9)_H$ and $(EA)_H$ respectively. Determine the register content after the execution of the following sequence of micro-operations sequentially.

i) A←A + B, C←C + shl(D)
ii) C←C ^ D, B←B + 1
iii) A←A – C
iv) A←shr(B)⊕cir(D)

b) With the help of neat block diagram explain the functioning of a Micro program Sequencer?

(10+8)

7. Write short note on **any three** of the following:

a) Booth Multiplication
b) Superscalar computers
c) Structural hazards and data dependence in Pipiline computer
d) Serial communication and parallel communication
e) Shared Memory architecture

(3x6)