

B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS

TOTAL MARKS: 100
(PART ONE – 40; PART TWO – 60)

PART ONE **(Answer all the questions)**

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1x10)**
 - 1.1 A combinational circuit which performs arithmetic addition of three bits is called
 - A) Half–adder
 - B) Full–adder
 - C) Double–adder
 - D) None of the above
 - 1.2 Storage capabilities are not provided in
 - A) ROM
 - B) RAM
 - C) Secondary Storage
 - D) None of the above
 - 1.3 ASCII is a _____ code
 - A) 6 bit
 - B) 7 bit
 - C) 8 bit
 - D) None of the above
 - 1.4 The transfer of information from a memory word to the outside environment is called
 - A) Read operation
 - B) Write operation
 - C) No operation
 - D) None of the above
 - 1.5 One bit in the instruction code may be used to
 - A) Distinguish between direct address and immediate address
 - B) Distinguish between indirect address and immediate address
 - C) Distinguish between direct address and indirect address
 - D) None of the above

- 1.6 The content of output bus is transferred into one of the registers in control unit of computer system by
- A) Decoder (destination selector)
 - B) ALU (operation selector)
 - C) Multiplexer (selector)
 - D) None of the above
- 1.7 In Hardware algorithm for multiplication, the sequence counter contains initially
- A) Multiplicand
 - B) Multiplier
 - C) The number of bits in multiplier
 - D) None of the above
- 1.8 In which method of asynchronous data transfer, source unit initiating the transfer does not know the actual receipt of the data by destination unit and similarly destination unit initiates transfer, does not know whether data has been placed on the bus.
- A) Strobe method
 - B) Handshake method
 - C) Serial asynchronous data transfer technique
 - D) None of the above
- 1.9 Reduced power consumption and larger storage capacity in single memory chip are characteristics of
- A) Static RAM
 - B) Dynamic RAM
 - C) ROM
 - D) None of the above
- 1.10 If CS contains '1ABCH' and IP contains '234EH', the address of the instruction to be executed is
- A) 1CF0EH
 - B) 03E0AH
 - C) 24F9CH
 - D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the “tear-off” sheet attached to the question paper, following instructions therein. (1x10)

- 2.1 Each combination of the variables in truth table is called minterm.
- 2.2 A decoder is a combinational circuit which converts binary information from n coded inputs to exactly 2^n unique output.
- 2.3 Addition of a positive number and a negative number may result overflow.
- 2.4 The input register INPR and output register OUTR communicate with communication interface serially and with accumulator AC in parallel.
- 2.5 PUSH and ADD are examples of Zero – Address Instruction.
- 2.6 Booth Multiplication algorithm uses binary integer in signed 2’s complementation form.
- 2.7 For handling Divide Overflow condition, additional flip flop is needed.
- 2.8 Each peripheral device has associated with it an interface unit.
- 2.9 Cache memory is placed between main memory and secondary memory.
- 2.10 Both segments register DS and ES point to the address of data.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1x10)

X		Y	
3.1	Subtraction of binary numbers is done using	A.	Read Only Memory
3.2	Time is same in locating a word in memory irrespective of its location.	B.	2’s complements
3.3	16^{th} complement of AB40 is	C.	Buffer gate
3.4	Used in design of bus system	D.	Divide overflow
3.5	OperandA OperandB *	E.	Multiplexer
3.6	Subtraction of two equal numbers in signed magnitude representation	F.	Random access
3.7	Quotient register fails to accommodate larger than largest quotient possible	G.	Reverse Polish notation
3.8	I/O processor	H.	54C0
3.9	ROM portion of main memory	I.	+0
3.10	Handling of all transfer of data and addresses on bus ((8086 machine)	J.	BIU
		K.	Bootstrap loader
		L.	Divide underflow
		M.	DMA

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1x10)

A.	Software	B.	Exclusive OR	C.	type
D.	Signed magnitude	E.	Counter	F.	De Morgan's
G.	I/O bus	H.	Op code	I.	Main memory
J.	Character	K.	Hardware	L.	String
M.	IP				

- 4.1 The invert – AND symbol for NOR gate follows from _____ theorem and from the convention that small circles denotes complementation.
- 4.2 A register which goes through a predetermined sequence of states upon application of input pulses is called _____.
- 4.3 The addition and subtraction operations can be combined into one common circuit by including _____ gate.
- 4.4 During time T₃, the control unit determines the _____ of instruction just read from memory in fetch – decode phase of instruction cycle.
- 4.5 _____ interrupt is initiated by executing an instruction.
- 4.6 The _____ representation of number may result two representations of zero.
- 4.7 _____ consists of data line, address lines and control lines.
- 4.8 Virtual memory system provides a mechanism for translating program generated addresses into correct _____ location.
- 4.9 The offset of instruction in CS is available at _____.
- 4.10 Extra segment (ES) is used in _____ instructions.

PART TWO
(Answer any **FOUR** questions)

- 5.
- a) Draw a block diagram of 4 – to – 1 multiplexer and explain its operations by means of function table.
 - b) Draw the logic diagram (using NAND gates) of S-R flip flop and give its truth table and characteristic table.
 - c) Perform arithmetic operation (+ 42) + (- 13) and (- 42) – (- 13) in binary using 2's complement representation for negative number.

(5+6+4)

- 6.
- a) What is half adder? Draw truth table and logic diagram of it. Explain how full adder is obtained using half adders by drawing logic diagram of it.
 - b) Write assembly language program segment / pseudo code to evaluate the following expression:

$$\frac{A + B * (C + D)}{E},$$

- using 0 – address instructions.
- c) Define addressing mode. Explain Immediate Addressing and Indirect Addressing mode with examples.

(8+3+4)

- 7.
- a) Draw the flow chart of Booth algorithm to multiply the number by a number in 2's complement. Explain the algorithm by using a numerical example by multiplying 9 by (-4).
 - b) Draw the diagram of DMA controller. Explain its working.

(8+7)

- 8.
- a) What is Virtual Memory? Give three reasons for using it.
 - b) Write an assembly language program to find the factorial of number given at NUM and the result is placed at RESULT. (Both NUM and RESULT are defined as word).
 - c) Write an assembly language program to count the number of full stop (.) in a message available at MSG which is of size of 100 characters.

(5+6+4)

- 9.
- a) What do you mean by Cache Memory? Explain direct mapping procedure used in cache memory.
 - b) What are the different addressing modes used in Basic Computer? Explain each to the point.

(9+6)