No. of Printed Pages : **3**

Sl. No.

C0-R4.B4 : COMPUTER SYSTEM ARCHITECTURE

NOTE :

1. Answer question 1 and any FOUR questions from 2 to 7.

2. Parts of the same question should be answered together and in the same sequence.

Time : 3 Hours **Total Marks : 100**

1. (a) Explain the addressing mode where the address of the operand lies inside the instruction.

(b) What is Cache coherency in multiprocessor environment ?

(c) Describe the following terminology associated with multiprocessors :

(i) mutual exclusion;

(ii) critical section;

(iii) hardware lock;

(iv) semaphore;

(v) test-and-set instruction.

(d) Differentiate between Tightly coupled multiprocessors and loosely coupled multiprocessors.

(e) How many 128*8 Ram chips are needed for a memory capacity of 2048 bytes ? How many lines of the address bus must be used to access 2048 bytes of memory ? How many of these lines will be common to all chips ?

(f) Differentiate between Isolated I/O and Memory mapped I/O.

(g) What are the drawbacks of Programmed driven I/O and how to resolve them ? **(7x4)**

2. (a) Using Restoring method, solve the following Dividend = 1011 and Divisor = 0011.

(b) How DMA transfer improves the speed of data transfer ?

(c) In a computer with cache, we have the average number of clock periods per instruction equal to 4, if there are no misses in the cache. What will be the real number of clock periods per instruction, if the probability of miss in the cache is 10% ?

(d) We want to speed up computer performance with an additional unit for calculating the floating point format. This unit is 20 times faster than the same operations without unit. What percentage of a total computer time must this unit be active to achieve an overall increase in computer speed for 2.5 times ? **(5+5+4+4)**

3. (a) Represent the number 85.125 in IEEE 754 floating point format (Single Precision).

(b) Convert the following numbers with the indicated bases to decimal numbers : $(12121)_3$; $(4310)_5$; $(50)_7$; and $(198)_{12}$.

(c) How the pipeline performance can be measured ? Discuss.

(d) Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

(i) How many bits are there in the operation code, the register code part, and the address part ?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory ?

(4+5+4+5)

4. (a) A ROM Chip of 1024*8 bits has four select inputs and operates from 5-volt power supply. How many pins are needed for IC package ? Draw block Diagram and label all inputs.

(b) A computer system has a 32-bit virtual address space with a page size of 8K, and 4 bytes per page table entry. How many pages are there in the virtual address space ? If the average process size is 1GB, would you use a one-level, two-level, or three-level page table ? Why ? What is the maximum size of addressable physical memory in this system ?

(c) Perform the required arithmetic operations needed in (i) and (ii) below. Represent the numbers as binary numbers and use signed 2's complement representation for negative numbers. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.

(i) $(+35)+(+40)$

(ii) $(-35)+(-40)$

(d) What is hardwired control unit ? Also explain linear and nonlinear pipeline processor.

(4+4+4+6)

5. (a) Starting from an initial value of R = 11011101, determine the sequence of binary values after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.

(b) Construct the bus system for four registers with the help of four 4*1 Multiplexers each having four data inputs (0 through 3) and two selection inputs (S1 and S2).

(c) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in 01101101 and 11111101.

(d) What is wrong with the following register transfer statements ?

(i) yT: R1 ← R2, R1 ← R3

(ii) zT: PC ← AR, PC ← PC

(3+4+5+6)

6. (a) How the Interrupts can be classified into various categories based on different parameters ?

(b) Describe MIPS R2000 instruction set in detail. Explain with examples.

(c) Discuss parallel processing. Describe various Flynn's Classification Instruction Set Architecture with the help of diagram. **(6+6+6)**

7. (a) Show the step-by-step multiplication process using Booth algorithm, when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers.

(i) $(+15) \times (+13)$

(ii) $(+15) \times (-13)$

(b) A binary floating-point number has seven bits for a biased exponent. The constant used for the bias is 64.

(i) List the biased representation of all exponents from -64 to $+63$.

(ii) Show that after the addition of two biased exponents it is necessary to subtract 64 in order to have a biased exponents sum. How would you subtract 64 by adding its 2's complement value ?

(iii) Show that after the subtraction of two biased exponents it is necessary to add 64 in order to have a biased exponent difference. **(9+9)**

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