Sl. No.

B1.4-R4 : COMPUTER SYSTEM ARCHITECTURE

अवधि : 03 घंटे **अधिकतम अंक : 100**
DURATION : 03 Hours **MAXIMUM MARKS : 100**

ओएमआर शीट सं. : **OMR Sheet No. :**					

रोल नं. : **Roll No. :**

उत्तर-पुस्तिका सं. : **Answer Sheet No. :**

परीक्षार्थी का नाम : **परीक्षार्थी के हस्ताक्षर :**
Name of Candidate : _____ **Signature of Candidate :** _____

परीक्षार्थियों के लिए निर्देश :	**Instructions for Candidate :**
कृपया प्रश्न-पुस्तिका, ओएमआर शीट एवं उत्तर-पुस्तिका में दिये गए निर्देशों को ध्यानपूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर दे सकता है।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** हैं। **भाग एक** में **चार** प्रश्न और **भाग दो** में **पाँच** प्रश्न हैं।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
भाग एक ''वैकल्पिक'' प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो** ''व्यक्तिपरक'' प्रकार का है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is Subjective type and carries 60 Marks.
भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई **ओएमआर उत्तर-पुस्तिका** पर, उसमें दिये गए अनुदेशों के अनुसार ही दिये जाने हैं। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the Question Paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात् दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the Answer Sheet for **PART ONE** is returned. However, Candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the Answer Sheet for **PART ONE** to the Invigilator.
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना और अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हॉल/कमरा नहीं छोड़ सकते हैं। ऐसा नहीं करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his/her Answer Sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात् एवं उत्तर लिखना आरम्भ करने से पहले उम्मीदवार जाँच कर यह सुनिश्चित कर लें कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before starting to answer the questions, the candidate should ensure that the Question Booklet is complete in all respect.

जब तक आपसे कहा न जाए, तब तक प्रश्न-पुस्तिका न खोलें।
DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE

(Answer ALL Questions; each question carries ONE mark)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10=10)

1.1 What is the minimum number of NAND gates required to construct XOR gate ?

(A) 5

(B) 4

(C) 3

(D) 6

1.2 1-bit adder can be implemented using _____ gate for sum and _____ gate for carry.

(A) NAND and AND

(B) EXOR and NAND

(C) EXOR and AND

(D) None of the above

1.3 In most of the digital computers, arithmetic operation of division is implemented with :

(A) Sequence of left shift micro-operations only

(B) Sequence of subtraction and left shift micro-operations

(C) Sequence of subtraction and right shift micro-operations

(D) None of these

1.4 _____ flip-flop is the refinement of the SR flip-flop in that indeterminate condition of the SR type is defined.

(A) JK flip-flop

(B) D flip-flop

(C) T flip-flop

(D) Edge triggered flip-flop

1.5 For direct addressing instruction _____ references to memory to fetch an operand are needed.

(A) Zero

(B) One

(C) Two

(D) Three

1.6 Stack memory is used in all data manipulation by :

(A) Two-address instruction

(B) Zero-address instruction

(C) One-address instruction

(D) Three-address instruction

1.7 Flag register holds the status of the :

(A) Arithmetic instruction

(B) Logical instruction

(C) Positive or negative number

(D) All of the above

1.8 For multiple I/O modules, how does the processor determines which device issued the interrupts ?

(A) Multiple interrupts lines

(B) Software poll

(C) Daisy chain

(D) All of the above

1.9 How many machine control flags are available in 8086 ?

(A) 0

(B) 1

(C) 2

(D) 3

1.10 The instruction -> Add LOCA, R0 does _____

(A) Adds the value of LOCA to R0 and stores in the temp register

(B) Adds the value of R0 to the address of LOCA

(C) Adds the values of both LOCA and R0 and stores it in R0

(D) Adds the value of LOCA with a value in accumulator and stores it in R0

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein.

(1x10=10)

2.1 Masking of bits are performed using AND Gate logic.

2.2 NAND gate can be used as the chip select for memory interface.

2.3 Minimum number of term in Boolean algebraic expression are obtained by DeMorgan theorem.

2.4 Don't care term is used to simplification of algebraic function.

2.5 In sequential circuit, the transition from present state to next state is activated by present of clock signal.

2.6 A decoder is the sequential circuit that converts binary information from the n code to maximum of 2^n.

2.7 2x4 decoder has 3 input in which two-bit is for selection line and two-bit for enable line.

2.8 Encoders are implemented using AND gate.

2.9 Binary counter can't be designed using T and J-K flip-flop because they can't complement the bit.

2.10 MOV AX, [BP] instruction of 8086 access data memory to move the 16-bit data to AX.

3. Match words and phrases in column X with the closest related meaning/word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10=10)

	X		Y
3.1	Carry into bit-4	**a.**	AND
3.2	Debugging Mode	**b.**	Flip-flops and gates
3.3	Masking operation	**c.**	Auxiliary Carry
3.4	Transfer of bits per second	**d.**	JK flip-flop
3.5	Code Segment memory offset	**e.**	Stack Segment
3.6	Sequential circuit	**f.**	Trap Flag
3.7	Output transition at specific level of clock pulse	**g.**	Baudrate
3.8	Base Pointer register	**h.**	IP
3.9	Stored Registers	**i.**	Buffering
3.10	Address bit	**j.**	Arithmetic Logic Shift unit
		k.	Latching
		l.	Edge-Triggered Flip Flop
		m.	Interrupt flag

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10=10)

(a)	Processor Bus	(b)	D Flag	(c)	Overflow flag
(d)	Multiplexer	(e)	IR	(f)	Flash Memory
(g)	144	(h)	MAR	(i)	150
(j)	Data path	(k)	PC	(l)	Control path
(m)	D flip flop				

4.1 The decoded instruction is stored in_____.

4.2 Which registers can interact with the secondary storage?

4.3 During the execution of a program, which is initialized first?

4.4 Pen drive is an example of _____.

4.5 The internal Components of the processor are connected directly by_____.

4.6 _____ is used to choose between incrementing the PC or performing ALU operations.

4.7 The registers, ALU and the interconnection between them are collectively called as _____.

4.8 _____ is used to store data in registers.

4.9 _____ flag bit is used for direction of memory increment and decrement in string instruction.

4.10 A decimal 100 is an equivalent of octal _____.

PART TWO

(Answer any Four questions)

5. (A) Simplify the following Boolean functions, using four-variable maps:

(i) $F(w, x, y, z) = \Sigma(1, 4, 5, 6, 12, 14, 15)$

(ii) $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 7, 11, 15)$

(iii) $F(w, x, y, z) = \Sigma(2, 3, 10, 11, 12, 13, 14, 15)$

(iv) $F(A, B, C, D) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

(B) Consider the following Boolean function, implement the circuit diagram by using multilevel NAND gate. F =(AB'+A'B).(C+D')

(C) Show that a JK flip-flop can be converted to D flip flop with inverter between the J and K inputs.

(5+5+5)

6. (A) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(B) How many lines of the address bus must be used to access 2048 bytes of memory ? How many of these lines will be common to all chips ?

(C) How many lines must be decoded for chip select ? Specify the size of the decoders.

(D) Draw the memory interface diagram for the above problem.

(3+3+2+7)

7. (A) Using booth algorithm of signed 2's complement multiplication perform the multiplication of $(-9) \times (-13)$.

(B) Explain the working of DMA (Direct Memory Access) transfer mechanism. **(8+7)**

8. (A) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

(B) Write an assembly language (8086) program to find the factorial of a number in Assembly Language.

(C) Differentiate between Programmed Driven I/O and Interrupt Driven I/O. **(5+5+5)**

9. (A) Explain memory hierarchy in detail.

(B) Explain Addressing modes in detail. **(8+7)**

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SPACE FOR ROUGH WORK

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