A4-R4: COMPUTER SYSTEM ARCHITECTURE

अवधि: 03 घंटे **अधिकतम अंक: 100**

DURATION: 03 Hours **MAXIMUM MARKS: 100**

ओएमआर शीट सं.: **OMR Sheet No.:**						

रोल नं.: **Roll No.:** | | | | | | |

उत्तर-पुस्तिका सं.: **Answer Sheet No.:** | | | | | | |

परीक्षार्थी का नाम: **परीक्षार्थी के हस्ताक्षर**:

Name of Candidate: _____; Signature of candidate: _____

परीक्षार्थियों के लिए निर्देश:	**Instructions for Candidate:**
कृपया प्रश्न-पुस्तिका**,** ओएमआर शीट एवं उत्तर-पुस्तिका में दिये गए निर्देशों को ध्यान पूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर दे सकता है।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** है। **भाग एक** में चार प्रश्न और **भाग दो** में पाँच प्रश्न है।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions**.**
भाग एक "वैकल्पिक" प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो**, "व्यक्तिपरक" प्रकार है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is subjective type and carries 60 Marks.
भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई **ओएमआर उत्तर-पुस्तिका** पर**,** उसमें दिये गए अनुदेशों के अनुसार ही दिये जाने है। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR.** Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE.**
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना एवं अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हाल नहीं छोड़ सकता हैं। ऐसा नही करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his Answer sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात एवं उत्तर देने से पहले उम्मीदवार यह जाँच कर यह सुनिश्चित कर ले कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before answering the questions, the candidate should ensure that the Question booklet is complete in all respect.

जब तक आपसे कहा न जाए तब तक प्रश्न-पुस्तिका न खोलें।

DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 The basic logic gates are
A) AND, NOR
B) NAND, inclusive OR (with multiple inputs)
C) AND, inclusive OR with multiple inputs and NOT (with single input)
D) None of the above

1.2 The smallest Signed number which can be accommodated in 2 byte register is
A) -2^{15} B) $-2^{15} - 1$
C) -2^{16} C) None of the above

1.3 The type of instruction is determined in 'Decode the Instruction' phase of Instruction Cycle by control unit during
A) Time T1 B) Time T2
C) Time T3 D) None of the above

1.4 If the second part of the instruction code specifies an operand, the instruction is said to have
A) Direct address B) Indirect address
C) Immediate address D) None of the above

1.5 The PUSH and POP instruction transfer data between processor registers and
A) Memory Word B) Memory Stack
C) System Registers D) None of the above

1.6 In non-vectored interrupt, the branch information (Branch address)
A) Is available at first address of I/O service routine.
B) Is an address which points to a location in memory where the beginning address of I/O service routine is stored?
C) Is assigned to a fixed location in memory.
D) None of the above

1.7 Multiprogramming means
A) Executing more than one program at same instant.
B) Existence of more than one program in ready to execute state in memory hierarchy at the same time.
C) Using more than one programming languages in a program
D) None of the above

1.8 Cache memory exploits
A) The stored program concept
B) The property of locality of reference
C) Properties of ROM
D) None of the above

1.9 System supporting Virtual memory means that
A) The computer system has capability to execute the program whose size is greater than the existing size of main memory
B) There also exists special type of memory
C) The system can store 3D images in memory
D) None of the above

1.10
```
MOV CX, 2
    MOV AX, 1
ONE:
    DEC CX
    LOOP ONE
```
In the above assembly program segment, how many times the loop ONE will be executed?
A) One time B) Two times
C) Zero time D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 OR gate may have more than one input.

2.2 The amount of electric power needed at the input of buffer is greater than the power produced at the output of the buffer.

2.3 In computer, the subtraction operation can be changed to an addition operation, if sign of subtrahend is changed.

2.4 Instruction code always specifies the operation requiring operands in the memory.

2.5 A hardware interrupt is initiated by executing an instruction.

2.6 Binary division is simpler than decimal division.

2.7 Strobe pulse method and hand shaking method of asynchronous data transfer are used only in I/O transfer.

2.8 Main memory of general purpose computer is made up RAM IC chip and ROM chip both.

2.9 Random memories are expensive in comparison to Associative memory.

2.10 CS (Code Segment) register of CPU holds tha base location of current executable instruction (code) in a program.

ROUGH WORK SPACE:

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	The small circle in output of the graphic symbol of inverter	**A.**	Binary adder
3.2	Complement of AND function	**B.**	Instruction pipeline
3.3	Digital circuit generating the arithmetic sum of two binary numbers of any length	**C.**	AH
3.4	Register containing the address of next instruction	**D.**	Mapping process
3.5	One of the arithmetic instruction	**E.**	Logic complement
3.6	Consecutive instructions are read from memory while previous instructions are being executed in other segment	**F.**	Bootstrap loader
3.7	Used to start computer operating system	**G.**	NAND
3.8	Time required to transfer data to or from device	**H.**	PC
3.9	Transforming of data from main memory to cache memory	**I.**	INC
3.10	Moving 126Fh to AX, results in 12h in which register of Assembly statement	**J.**	Transfer time
		K.	NOR
		L.	IR
		M.	JMP

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Choose the most appropriate option, enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	AX	**B.**	Indeterminate	**C.**	16
D.	Hit ratio	**E.**	AC	**F.**	Synchronous
G.	Address space	**H.**	Cycle stealing	**I.**	Inverter
J.	Seek time	**K.**	Memory space	**L.**	In IEEE format
M.	Parallel				

4.1 _____ circuit inverts the logical sense of binary system.

4.2 In Hexadecimal number system _____ distinct characters are used to form this number.

4.3 Input and output instruction are also needed for transferring information to and from _____ register.

4.4 In three – state gate, besides two states 0 and 1, the third state is _____ - state.

4.5 Internal interrupt is _____ with the program.

4.6 _____ allows DMA controller to transfer one data word at a time after which it must return control of the buses to the CPU.

4.7 Time required to position read – write head to location is called _____.

4.8 The high _____ verifies the validity of the locality of reference property.

4.9 The set of addresses used by a programmer in Virtual memory system is known as _____.

4.10 Register _____ is called accumulator register.

ROUGH WORK SPACE:

PART TWO
(Answer any FOUR questions)

5.

a) What is decoder? Draw the logic diagram of 2-to-4 line decoder with an enabled input constructed with NAND gates and its truth table.

b) What is Multiplexer? Draw logic diagram and function table of 4-1 line multiplexer. How many rows will be there in the truth table describing the 4-1 multiplexer circuit and why?

(7+8)

6.

a) i) Add (1FFE) + (123A) =
   ii) Write the sum of i) in binary and give its 2's complement also.

b) Write a program to evaluate the arithmetic statement:
   X = ((A – B) + (C*D)) / (E + F * G)
   i) Using a general register computer with two address instructions.
   ii) Using an accumulator type computer with one address instruction.

(7+8)

7.

a) Write an assembly language program segment to add 15 numbers which are given as words at NUM. Put the sum at SUM.

b) What is difference between a direct and indirect address instruction? How many reference to memory are needed for each type of instruction to bring an operand into a process register?

c) A computer uses a memory unit with 512K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four part: an indirect bit, an operand code, a register code part to specify one of 16 registers and an address part.
   i) How many bits are there in operation code, the register code part and address part?
   ii) Draw the instruction word format and indicate the number of bits in each part.
   iii) How many bits are there in the data and address inputs of the memory?

(5+6+4)

8.

a) Explain the Booth multiplication algorithm using the flow chart and use this algorithm to multiply (-3) by (-9).

b) What is advantage of interrupt initiated I/O. Differentiate between vectored interrupt and non-vectored interrupt.

(8+7)

9.

a) What is DMA? How is CPU placed in idle state? Explain DMA controller through block diagram.

b) What is Cache Memory? How does it work? How its performance measured? Explain direct mapping of cache memory.

(8+7)

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ROUGH WORK SPACE:

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