C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram?

b) What must be the address field of an indexed addressing instruction to make it the same as a register indirect mode instruction?

c) What is the difference between a software interrupt and a subroutine call?

d) Define microoperation.

e) Give four peripheral devices that produce an acceptable output for a person to understand.

f) List various cache mapping schemes. Explain any one in detail.

g) Describe mutual exclusion and critical section in context with multiprocessors.

(7x4)

2.

a) A fixed-point binary number system has 1 whole bit and 15 fractional bits.

i) What is the range of numbers represented, assuming an unsigned format?

ii) What is the range of numbers represented, assuming 2's complement format?

iii) Represent the decimal fractions 0.75 and 0.3 in the format of **part i)**.

b) Assume single precision FP numbers as x = z = $1.0 * 2^0$ and y = 2^{-25}. Compute (x + y) – z with round-to-nearest-even mode. Why the exact mathematical result differs from FP result?

c) What is the radix of the numbers if the solution to the quadratic equation $x^2 - 10x + 31$ is $x = 5$ and $x = 8$?

(6+6+6)

3.

a) Write a program in assembly language to evaluate the expression X = (A – B + C * (D * E – F)) / (G + H * K).

i) Using a general register computer with two address instructions.

ii) Using a stack organized computer with zero-address instruction.

b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

i) How many bits are there in the operation code, the register code part, and the address part?

ii) Draw the instruction word format and indicate the number of bits in each part.

iii) How many bits are there in the data and address inputs of the memory?

(9+9)

4.

a) What is wrong with the following register transfer statements?

i) xT: AR ← ARbar , AR ← 0

ii) yT: R1 ← R2, R1 ← R3

iii) zT: PC ← AR, PC ← PC + 1

b) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

i) How many selection inputs are there in each multiplexer?

ii) What sizes of multiplexers are needed?
iii) How many multiplexers are there in the bus?

c) Represent the following conditional control statement by two registers transfer statements with control functions.
If (P = 1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3)

(6+6+6)

5.

a) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques.

b) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process the eight tasks.

c) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum speed-up that can be achieved?

(6+6+6)

6.

a) What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without an interrupt?

b) A data communication link employs the character controlled protocol, with data transparency using the DLE character. The text message that transmitter sends between ETX and STX is as follows:
DLE STX DLE DLE ETX DLE DLE ETX DLE ETX
What is the binary value of transmitted text data?

c) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?

(6+6+6)

7.

a) An address for a byte-addressable memory presented to the cache unit is divided as follows: 13-bit tag, 14-bit line index, 5-bit byte offset.
i) What is the cache size in bytes?
ii) What is the cache mapping scheme?
iii) For a given byte in cache, how many different bytes in the 2^{32}-byte main memory can occupy it?

b) A computer has a cache, main memory, and a disk. If a referenced word is in the cache, 20 ns are required to access it. If it is in the main memory but not in the cache, 60 ns are required to load it into the cache, and then the reference is started again. If the word is not in the main memory, 12 ms are needed to load it from the disk to main memory, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main memory hit ratio is 0.6. What is the average time needed to access a referenced word?

c) A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table consists of the following entries:

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by CPU.

(6+6+6)