CO-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Define MIPS and MFLOPS. How they contribute in measuring the speed of CPU?

b) Define execution time and throughput.

c) Differentiate between hardwired and micro programmed control unit.

d) Define micro operation.

e) Explain the principle of locality of reference.

f) List various cache mapping schemes. Explain any one in detail.

g) Differentiate between isolated vs Memory mapped I/O.

(7x4)

2.

a) What is the significance of addressing modes? Differentiate between direct and indirect addressing modes? Explain the implied mode, immediate mode and register mode of addressing in detail.

b) A 32 bit computer has two selectors channels and one multiplexer channel. Each selector channel supports two magnetic disks and two magnetic tape units, the multiplexer channels has two line printers, two card readers and 10 VDT terminals, connected to it. Assume the following transfer rates,

Disk drive: 800 Kbytes

Magnetic Tape drive 200 Kbytes

Line printer 6.6 Kbytes

Card reader 1.2 Kbytes

VDT 1 Kbytes

Estimate the maximum aggregate I/O transfer rate in this system.

(9+9)

3.

a) What is meant by virtual address? What are the various steps of virtual address translation?

b) List various page replacement policies. Explain them in detail with suitable example.

c) With the help of block diagram, explain the concept of direct memory transfer.

(6+6+6)

4.

a) List the basic functionalities of shift register. Make the diagram of general purpose shift register and explain it's functioning.

b) The following transfer statements specify a memory. Explain the memory operation in each case.

i) $R2 \leftarrow M[AR]$

ii) $M[AR] \leftarrow R3$

iii) $R5 \leftarrow M[R5]$

c) Draw the block diagram for hardware that implements the following statements

$x+yz : AR \leftarrow AR + BR$

where AR and BR are two n bit registers and x, y, z are control variables. Include the logic gates for control functions.

(6+6+6)

5.

a) The following control inputs are active in the bus system shown below: For each case, specify the register transfers that will be executed during next clock transition.

	S2	S1	S0	LD of register	Memory	Adder
a.	1	1	1	IR	Read	--
b.	1	1	0	PC	--	--
c.	1	0	0	DR	Write	--
d.	0	0	0	AC	--	Add

b) Consider the situation, in which, the contents of AC in basic computer is hexadecimal A937 and the initial value of E is 1. Determine the contents of AC, E, PC, AR and IR in hexadecimal after the execution of CLA instruction.

c) Make the flow chart of Booths algorithm for multiplication. Show the steps of multiplication of calculation 1110 X 1010.

(6+6+6)

6.

a) A CPU with a 20 MHz clock is connected to a memory unit, whose access time is 40 ns. Formulate 'read' and 'write' timing diagram, using READ strobe and WRITE strobe include the address in timing diagram.

b) A data communication link employs the character controlled protocol, with data transparency using the DLE character. The text message that transmitter sends between ETX and STX is as follows:

DLE STX DLE DLE ETX DLE DLE ETX DLE ETX

What is the binary value of transmitted text data?

c) An 8 bit computer has a 16 bit address bus, the first fifteen lines of address are used to select a bank of 32 K Bytes of memory. The higher order bits of the address is used to select a register which receives contents of data bus. Explain how this configuration can be used to extend the memory capacity of system to 8 banks of 32 K Bytes each, for a total of 256 K bytes of memory.

(6+6+6)

7.

a) An address space is specified by 24 bits and corresponding memory space by 16 bits.
   i) How many words are there in memory space?
   ii) If a page consist of 2K words, how many pages and block are there in the system?

b) The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are read and remaining 20% for write. This hit ratio for read access only is 0.9. A write through procedure is used.
   i) What is the average access time of the system considering only memory read cycles?
   ii) What is the average access time of the system for both read and write requests?
   iii) What is the hit ratio taking into consideration the write cycles?

c) A virtual memory has a page size of 1 K words. There are 8 pages and four blocks. The associative page memory table consists of following entries:

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses, that will cause a page fault, if used by CPU.

(6+6+6)