B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

IMPORTANT INSTRUCTIONS:

1.   There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2.   **PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3.   Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1.   **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein.   (1x10)**

1.1   Decoder is a _____
A)   Multiple input multiple output logic
B)   Single input multiple output logic
C)   Multiple input single output logic
D)   Single input single output logic

1.2   A 2^N encoder will generate _____ outputs
A) 2^N outputs
B)   n outputs
C)   log n outputs
D)   n logn outputs

1.3   Half adder can be implemented using _____
A)   OR and AND GATE
B)   NAND and AND GATE
C)   XOR and AND GATE
D)   None of the above

1.4   PLC stands for _____
A)   Program logic code
B)   Programmable logic device
C)   Performance logo code
D)   Programmable light contact

1.5   The function of system bus is _____
A)   to carry control signals between CPU and main memory.
B)   to carry address between Virtual memory and main memory
C)   to carry data between keyboard and printer
D)   none of the above

1.6   MIPS is defined as _____
A)   (CPI) / Clock rate
B)   Clock rate / (CPI)
C)   1/execution time
D)   Execution time / CPI

1.7   The Octal equivalent of the Hexa Decimal number A277 is
A)   121167
B)   504731
C)   5277
D)   7725

1.8   ALU works for
A)   Executing the instructions,
B)   Performing the data transfer
C)   Memory storage
D)   None of the above

1.9   DMA stops further transfer when
A)   control register contains zero
B)   address register contains zero
C)   word count register contains zero
D)   control register contains one

1.10   Instruction Fetch stands for _____
A)   Transfer of instruction from memory to IR
B)   Transfer of instruction from keyboard
C)   Transfer of instructions to display
D)   None of the above

2.   Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein.   (1x10)

2.1   Cache memory is content addressable.

2.2   SR flip flop has a race condition problem.

2.3   Cross assembler generates machine language for different types of computers.

2.4   Debugger is used to find and fix errors.

2.5   In assembly language   DW directive stands for Define Width.

2.6   Code segment is used for storing user Program.

2.7   The total memory of 8086 is 1 MB.

2.8   In immediate addressing mode data is provided in the instruction itself.

2.9   ISR stands for Interrupt Service Routine.

2.10   Instruction MVI A,30 H has implied addressing mode.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

	X		Y
3.1	Flip flop has	**A.**	Can shift its stored data by one bit position at each clock period
3.2	Shift register	**B.**	2 stable states
3.3	N bit counter	**C.**	Is made up of MOS transistors gates
3.4	Dynamic Ram	**D.**	Increments to its own value on each clock cycle.
3.5	Instruction Set Architecture	**E.**	32 instruction
3.6	6 bit operand can support	**F.**	1024 K bytes
3.7	The capacity of 20 bit address memory is	**G.**	Deals with functional behavior of a computer system as viewed by programmer
3.8	Throughput is defined as	**H.**	Number of tasks completed per unit time.
3.9	Number of select lines in 8to 1 multiplexer is	**I.**	Effective address
3.10	Target instruction in branch type instruction is	**J.**	3
		K.	1024 Bytes
		L.	64 instruction
		M.	6

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	8 bits	**B.**	MIPS	**C.**	Macroprogramming
D.	Compiler	**E.**	Sign bits and exponents and mantissa	**F.**	Instruction register
G.	2's complement	**H.**	Register Transfer Language	**I.**	7 bits
J.	Asynchronous system.	**K.**	Microprogramming	**L.**	Register
M.	Microoperations				

4.1 The micropogammed control unit is implemented with _____.

4.2 _____ converts high level language to machine level language.

4.3 Language that is generated by transfer of signals between registers is called as _____.

4.4 Logic _____ can be used to manipulate individual bits.

4.5 _____ is the register that stores the instruction.

4.6 _____ is the speed measurement parameter for computer.

4.7 _____ is a method to represent negative numbers.

4.8 Digital circuits where no single indication of when to change the state is known as _____.

4.9 For a computer with instruction set size of 200, the opcode size is _____.

4.10 Components of a typical IEEE floating point numbers are _____.

PART TWO
(Attempt any **FOUR** questions)

5.
a)   List any 4 arithmetic micro operations and describe their functionality.
b)   Make the circuit diagram of 4:1 multiplexer and explain its operation.

                                                                                                    (8+7)

6.
a)   Assume cache miss rate of 5%with cache memory of 20 nsec cycle time and main memory of
      150 nsec cycle time. Calculate average cycle time.
b)   What is cycle stealing? How is data transferred from DMA?
c)   A computer has 64 K word memory. A computer uses 2 way associative caches with a capacity
      of 128 words each cache block contains8 words calculate the number of bits in the TAG, SET
      and WORD field of main memory address.

                                                                                                    (5+5+5)

7.
a)   Draw flow chart for Booth Algorithm for multiplication of signed 2's complement numbers and
      explain step by step multiplication of (-8) and (-12).
b)   Explain the working of Virtual memory.

                                                                                                    (10+5)

8.
a)   Write an assembly language code to   multiply two 8 bit numbers.
b)   What is meant by Page replacement? Explain any 3 page replacement algorithms in detail.

                                                                                                    (10+5)

9.
a)   Draw and explain 4-bit adder-subtractor circuit.
b)   Explain any two addressing mode with suitable example.

                                                                                                    (10+5)