C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What are the differences between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

b) What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors?

c) Draw a flowchart for interrupt cycle.

d) What are the basic differences between a branch instructions, a call subroutine instruction, and program interrupt?

e) Consider the multiplication of two 40×40 matrices using a vector processor,

(i) How many product terms are there in each inner product, and how many inner products must be evaluated?

(ii) How many multiply-add operations are needed to calculate the product matrix?

f) Why does DMA have priority over the CPU when both request a memory transfer?

g) A computer employs RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

i) How many RAM and ROM chips are needed?

(7x4)

2.

a) The outputs of four registers, R0, R1, R2 and R3 are connected through 4-to-1-line multiplexers to the inputs of a fifth register, R5. Each register is eight bits long. The required transfers are dictated by four timing variable T_0 though T_3 as follows:

$$T_0 : R5 \leftarrow R0$$
$$T_1 : R5 \leftarrow R1$$
$$T_2 : R5 \leftarrow R2$$
$$T_3 : R5 \leftarrow R3$$

The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of register R5.

b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	D = A + B (add)	D = A + 1 (increment)
1	D = A – 1 (decrement)	D = A + $\overline{B}$ + 1 (subtract)

c) The 8-bit registers AR, BR, CR and DR initially have the following values

AR = 11110010
BR = 11111111
CR = 10111001
DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

AR ← AR + BR	Add BR to AR
CR ← CR ∧ DR, BR ← BR + 1	AND DR to CR increment BR
AR ← AR – CR	Subtract CR from AR

(6+6+6)

3.

a) A computer uses a memory of 65,536 words eight bits in each word. It has the following registers; PC, AR, TR (16 bits each), and AC, DR, IR (eight bits each). A memory-reference instruction consists of three words: an 8-bit operation-code (one word) and a 16-bit address (in the next two words). All operands are eight bits. There is no indirect bit.

i) Draw a block diagram of the computer showing the memory and registers (Do not use a common bus).

ii) Draw a diagram showing the placement in memory of a typical three word instruction and the corresponding 8-bit operand.

iii) List the sequence of microoperations for fetching a memory reference instruction and then placing the operand in DR. Start from timing signal T_0.

b) Write subroutine to subtract two numbers. In the calling program, the BSA instruction is followed by the subtrahend and minuend. The difference is returned to the main program in the third location following the BSA instruction.

(9+9)

4.

a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?

b) Discuss the purpose of each register used in DMA controller.

c) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.

d) Enumerate the advantage of multiprocessing.

(4+4+6+4)

5.

a) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

b) Perform the arithmetic operations below with binary numbers and with negative numbers in signed-2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.

i) (+35) + (+40)

ii) (-35) + (-40)

c) Formulate a hardware procedure for detecting an overflow by comparing the sign of the sum with the signs of the augends and addend. The numbers are in signed-2's complement representation.

(4+6+8)

6.

a) Derive an algorithm flowchart form for adding two fixed point binary numbers when negative numbers are in signed-1's complement representation.

b) Show that 673 – 356 can be computed by adding 673 to the 10's complement of 356 and discarding the end carry. Draw the block diagram of a three-stage decimal arithmetic unit and show how this operation is implemented. List all input bits and output bits of the unit.

c) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?

(4+8+6)

7.

a) Explain the basic operation of a cache memory. How does a performance of cache memory measured?

b) Draw a block schematic of multiport memory system for 4 CPUs and 4 memory modules. Explain its working. What is the advantage of multiport memory organization?

c) Using a set of identical processing elements each having a local memory, draw a figure of SIMD array processor organization and explain its working.

(6+6+6)