COURSE PROSPECTUS

Name of the Group: *VLSI DESIGN GROUP*

Name of the Course: Advanced Diploma - *VLSI Physical Design Engineer*

Course Code: *VL701*

Starting Date: *07-Oct-2015*

Duration: *3 months(400 Hours)*

Preamble: VLSI (Very Large Scale Integration) technology has emerged as a very important technology in modern electronics featuring deep sub-micron manufacturing processes, low voltage operations, exploding speeds and smart programmable devices sufficient enough to digest ambient conditions to extremes. The electronics industry worldwide is rapidly approaching another revolutionary leap in the global market scenario. Semiconductor technology has crossed the quarter-micron threshold, making tens of millions of transistors available on a single chip equipped with the powerful arm of VLSI design. This imparts the electronics industry a potential to create designs of incredible densities and lightning speeds while utilizing batteries to power them. This has had a phenomenal impact on widespread applications ranging from consumer electronics, communications, and defense to just about everything.

As part of Electronics India program by Govt. of India, most of the electronic products and semiconductor ICs are planning to make in India. This skill development program in VLSI Physical design will help to generate skilled manpower in IC design and manufacturing.

Objective of the Course:

It is proposed to offer ***Advanced Diploma in VLSI Physical Design Engineer*** *to enable new Electronics graduates/post graduates or working engineers in electronic industries to the concepts used in IC Design, which involves processing, Layout, System Design Methods using Cadence tool. The course will benefit VLSI Engineers seeking lateral shift to a back end job. Engineers looking to work for Block level Physical Design Implementation, Place and Route job domains. This will take VLSI Engineers to a new level known as Physical Design Engineer. The Physical Design Engineer is responsible for converting the circuit design to a geometric representation for manufacturing the integrated circuit (IC).*

The main objective of the course is to make individuals understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout

During course work, each individual will get ample time to practice the theory taught in class in the lab sessions.

Outcome of the Course: After successful completion of the course individuals will understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout. The course will also help to fetch VLSI Physical Design job for job seekers in VLSI area.

Course Structure:

VL701	***Module name***	***Duration***
Module 1	*Introduction to IC Design Flow*	*1 weeks*
Module 2	*Basic CMOS Digital IC Design*	*2 weeks*
Module 3	*Processing and Layout*	*2 weeks*
Module 4	*System Design and Design Methods*	*2 weeks*
Module 5	*Analog IC Design*	*2 weeks*
	Project	*3 weeks*

Other Contents

a. Course Fees :
General Category applicants: ***Rs 30000/- + Service Tax at Actual***

SC/ST Category applicants : Tuition fees/Examination fees are waived for SC/STstudents admitted under SCSP/TSP. However they are required to remit an amount of Rs 3420/- as advanced deposit and this amount will be considered as caution/security deposit and will be refunded after successful completion of the course. If the student fails to complete the course successfully this amount along with any other caution/security deposits by the student will be forfeited.

b. Course Fee Installment Structure:

1. Deposit at the time of Course Registration of Rs.1000/- will be considered as caution deposit on student joining the course.

2. Fee Installment structure for PG/Advanced Diploma programs is as follows:

Advance Deposit :
Rs.10,000/- for PG Diploma Programs.

Rs.5,000/- for Advanced Diploma Programs.

(After publication of first selection list, the students in the first selection list have to pay the advance Deposit within one week to take the provisional admission. Students in the additional selection should pay both Advance and First installment fee together on or before counseling day)

First Installment:
50 % of Course fee (which includes advance deposit of Rs.10,000/- or Rs.5,000/- depending upon the type of course) + Service tax at actual. First installment should be paid on or before Counseling date.

Second Installment:
Remaining 50% of Course fee + Service tax at actual. Second Installment should be paid within two months after commencement of the course.

3. SC/ST Candidates should pay 10% of total fee as Advance deposit for taking provisional admission. This amount will be considered as caution/security deposit and will be refunded after successful completion of the course. If the student fails to complete the course successfully this amount along with any other caution/security deposits by the student will be forfeited, subject to approval of Director on case to case basis.

For Advanced Diploma - *VLSI Physical Design Engineer* the fee payment structure is as follows

Advance Deposit : Rs.5,000/- only (Should be paid within one week of first selection list)
1st Installment on or before counseling Date : Rs.15,000/- Plus Service Tax* = Rs.17100/- [Rs.5,000/- already paid] Net Amount Payable = Rs.12100/-
2nd Installment : Rs.15,000/- Plus Service Tax* = Rs.17100/- (Should be paid within one month after commencement of Course)
SC/ST Candidates need to pay only Rs 3420/- as advanced deposit and this amount will be considered as caution/security deposit and will be refunded after successful completion of the course.

* Service Tax is presently 14.0% and revised rates are applicable as per Govt of India Orders.

a. Eligibility: M.E/ M.Tech/ B.E/ B.Tech/ M.Sc in Electrical/ Electronics and Communication/ Electronics and Instrumentation/ Computer Science and allied branches.

b. Number of Seats : *15*

c. How to Apply :

Students are advised to apply in the prescribed Application Form available with the course brochure/course prospectus or downloaded from our website. Filled-in application forms along with a Demand Draft (or pay-in-slip) towards advance fee of Rs.1,000/- *drawn in favour of* Director, NIELIT, Calicut, *Payable at* State Bank of India, NIT Campus Branch (code: 2207), Chathamangalam should be sent to the **Training Officer, NIELIT, P. B. No. 5, NIT Campus Post, CALICUT – 673 601, Kerala**. **The Name of the Course Applied for should be super scribed on the top of the cover in which the application form is forwarded.**

Modes of Payment: The course fee can be paid by one of the following methods as per your convenient.

1	Demand Draft to be drawn in favor of Director, NIELIT, Payable at State Bank of India, Calicut NIT Branch (2207). The DD should reach here before the last date to apply.
2	Through any branch of SBI (where this format is accepted) using the pay in slip available in our web site. The **original counterfoil** should reach here before the last date to apply.
3	The fees can be paid directly into our account from any bank where core banking facility is available. The details required for direct payment are as given below. • Savings Account No: **31329537747** • Bank Name: SBI, NIT Chathamangalam • Bank Code: 2207 • IFSC No: SBIN0002207 • MICR : **673002012** The depositor should obtain the UTR Number/Journal No from the branch while depositing cash directly into our account. Depositor should also obtain the counterfoil duly filled up and signed by the staff with seal of the bank through which the amount was deposited. The following details should reach here before the last date to apply. 1. Name of the Depositor 2. Name of the Student 3. Date of Payment 4. Amount Deposited 5. Name of Bank/branch through which amount deposited 6. Purpose – Course ID – Advance Deposit/Hostel Rent/Installment Fee etc. 7. Proof of Deposit (counterfoil/acknowledgement **in original**) 8. UTR Number
4	The fees can be paid through the **SBI Collect** Payment Gateway as well: 1. Please click the SBI Collect hyper link to enter the payment gateway. 2. Select State of Corporate/Institution as *Kerala*

	3. *Select* Type of Institution *Educational Institutions* and click on *Go* button 4. *Select* Educational Institutions Name as *NIELIT* and click *Submit* button 5. Select Payment Category as *Course Fee* 6. Enter all the fields including amount payable and follow the instructions The following details should reach here before the due dates. 1. Name of the Depositor 2. Name of the Student 3. Date of Payment 4. Amount Deposited 5. Purpose – Course Name: 6. UTR Number

The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

c. Selection of candidates : Candidates will be selected based on the marks in the qualifying degree.

d. Test/Interview (if applicable) : Not Applicable

d. Counseling/Admission : on 05/10/2015 and 06/10/2015

e. Spot Admission : If spot admission is open, spot admission will close within 15 days of Counseling/Admission of a particular course. On spot admission students should provide an undertaking saying that he/she is fully aware that he/she missed so much days of class and will not ask for further extension of course.

f. Admission Procedure :
Students who have been selected for test/interview/counseling/admission are required to report to the Institute on the prescribed day by 9:30 hrs along with the following
1. Attested Copies of Proof of Age, Qualifications, etc
2. Original Certificate of the above
3. Two copies of photograph and one stamp size photograph for identity card.
4. SC/ST Certificate (if applicable)
5. Income Certificate (if applicable)
The students on reaching the Institute are required to meet the Front Office Councilor (FOC). The FOC then directs the student to the Course Coordinator. The student gets the enrollment form verified by the Course Coordinator and then meets the FOC who shall direct the student to the Accounts for payment of fees. A student is thus admitted.

g. Discontinuing the course: No fees under any circumstances shall be refunded in the event of a student discontinuing the course. A student can however, be eligible

for module certificates (applicable only for courses which provide for modular admission) which he has successfully completed provided he has paid the entire course fees.

Course Timings : Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm).

h. Location and how to reach :
NIELIT Calicut is located very close to NIT campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses (Buses to NIT via Kunnamangalam) are available from "Palayam Bus Stand and KSRTC Bus Stand". The bus stop at our Institute is called "Panthrand" and is one stop before NIT. The bus fare is around *Rs.17/-* from Calicut City to NIELIT.

Calicut (Kozhikode) is well connected by Rail, Road and Air form different parts of the country. The maximum and minimum temperatures range between 35^0C and 20^oC.

i. Course enquiries :
Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm).

Important Dates (if applicable) :

Last date for receiving completed application forms	First selection list will be prepared based on the applications received on or before 04th Sept 2015. The additional selection list will be prepared based on the applications received on or before 25th Sept 2015, and excluding the applicants, included in the first selection list.
Publication of first selection list in the Website http://calicut.nielit.gov.in/	7th Sept 2015
Last date for taking provisional admission by paying Advance Deposit (Rs 5000/-), for applicants in the first selection list	14th Sept 2015
Publication of additional selection list in our website (if there are vacant seats)	28th Sept 2015
Counseling date	05th and 6th Oct 2015
Class Commencement date	07th Oct 2015
Payment of Advance Deposit (Rs 5000/-) for applicants in first selection list	On or before 14th Sept 2015
Payment of first installment fees	On or before 05th Oct 2015
Payment of second installment fees	On or before 09th Nov 2015

j. Placement : We have a placement cell, which provides placement assistance to students who qualify our courses. The course improves the knowledge and skill of

the students as it deals with the latest technologies and tools used in industries. This helps the student in getting a placement by

a. Campus placement
b. Placement by companies for whom we send the students bio data and they conduct interviews at their site.
c. Students themselves attend interview at different companies and the course helps in the interview.

k. Hostel facilities :

Hostel accommodation is available for boys and girls on daily or monthly chargeable basis. *The hostel fee varies from Rs.850/- to Rs.1,300/- (for boys) per month and Rs.1,000/- to Rs.1,400/- (for Girls) per month depending on the location of accommodation.* However, students are required to pay the hostel fees for the duration of the course for which they are seeking admission at the time of joining the course.

l. Canteen facilities :

The Institute has a canteen functioning at the main campus and food at reasonable rates is available for breakfast, lunch, and dinner

m. Lab Facilities :

Full-fledged lab with CADENCE and Mentor Graphics ASIC Frontend and Backend Design Tools, High-end FPGA based embedded development boards, Digital Storage Oscilloscopes, SMD soldering station, High Precision Digital Multimeters, Xilinx, Altera and Mentor Graphics FPGA & PLD design tools, FPGA & PLD based Demo boards, PCB design tools such as OrCAD Capture, OrCAD PCB Layout Plus, OrCAD Digital Simulator, etc.

HARDWARE

- Xilinx FPGA Development Boards(Virtex 6,Spartan 6,Virtex 2,Spartan 3,Spartan 2 etc)
- Altera Development Boards(Stratix II,Cyclone IV,III,II etc)
- PSoC Development Boards from Cypress Semiconductor
- Ultrasound Trasmitter,Reciever Boards
- Logical Analyzer,CROs,Power Supplies,Testing Equipments
- SMD Soldering Station

SOFTWARE

- Mentor Graphics
- Cadence Tool Suite for ASIC Frontend and Backend
- MATLAB
- Xilinx ISE
- Altera Quartus
- PSoC Creator

n. Course Contents :

Core Modules

Module 1:-Introduction to IC Design Flow

ASIC Design Concepts, ASIC Design Flow-Frontend and backend, EDA tools for Frontend and backend, Introduction to Verilog HDL, Hardware Modeling Overview.

Module 2:- Basic CMOS Digital IC Design

CMOS Logic Design: MOS Fundamentals, MOS switches and design, Transmission Gates, CMOS Inverter Characteristics, CMOS Combinational and sequential logic. Introduction to IC Layout, IC Layout Design tools, RTL to GDSII, Introduction to Physical Verification (DRC, LVS, SoftCheck, Antenna and DFM)

Module 3:- Processing & Layout

Silicon semiconductor technology: an overview. CMOS fabrication flow, Process Gradient effects, Deep-Sub Micron Short channel effects and matching concepts. CMOS technologies, Layout design rules, Process parameterization. CMOS circuit Characterization and performance estimation. Circuit examples.

Module 4:- Systems Design and Design Methods

Chip level and block level implementation steps, Floor plan and power planning, Placement and clock tree synthesis, Routing, Physical Verification and DFM Checks, Signal integrity and back annotation, Sign off Checks and Tape out/Handoff. CMOS Subsystem design- SRAM and ALU.

Module 5:- Analog IC Design

Full custom IC Design flow. Simple Analog Circuits. Analog Layout considerations- Transistor layout, Capacitor Matching, Resistance layout, noise considerations. Complex analog circuit design example. Introduction to Analog mixed signal design. Analog and mixed signal building blocks, Layout concepts, Matching, Symmetry routing, Device placement layout techniques and Physical verification. ERC and Density check.

Module 1	Introduction to IC Design Flow	1 week
Module 2	Basic CMOS Digital IC Design	2 weeks
Module 3	Processing & Layout	2 weeks
Module 4	Systems Design & Design Methods	2 weeks
Module 5	Analog IC design	2 weeks
	Project	3 weeks