National Institute of Electronics &
Information Technology Near IIT Patna,
Amhara, Bihta, Patna(Bihar) -801106

Name of the Course: - Industrial Training & Internship in VLSI Design

---

Duration: 40 Hours / 4 Weeks
Course Fee: Rs. 1,983/-
Eligibility Criteria: B.E./B.Tech students in ECE/EE/CS/IT/EI or related fields/B.Sc. (Electronics/IT), M.Sc. (Electronics/IT)/Diploma holders (2 years) after 12th in ECE/EEE/CS/IT

Registration Link: http://nielitpatnaonline.in/

Objective of the Course

This course aims to provide a **comprehensive understanding of RTL (Register Transfer Level) design**, covering **basic to advanced concepts**. Participants will learn about **digital design, Verilog/VHDL programming, synthesis, and static timing analysis (STA),** using **Synopsys tools**. Hands-on experience will enable students to implement **real-world RTL designs** and prepare for careers in **semiconductor and ASIC/FPGA industries**.

Prerequisites

- A computer/laptop with at least **4 GB RAM (preferably higher) and a 2 GB Graphics Card**
- Stable internet connection (**2 Mbps or higher recommended**)
- **Basic knowledge of Digital Electronics and Logic Design**
- Familiarity with **Verilog/VHDL and simulation tools** is an advantage

---

Course Outcomes

Upon completion of this course, participants will be able to:

1. Understand **RTL design methodologies and processes**
2. Develop and optimize **RTL code for ASIC/FPGA designs**
3. Implement **logic synthesis using Synopsys Design Compiler**

Course Structure

Module No	Module Title	Duration (Hours)
1	Fundamentals of RTL Design	10
2	Verilog/VHDL Programming	15
3	RTL Coding Guidelines & Best Practices	10
4	Synthesis using Synopsys Design Compiler	5
Total	**Course Duration**	**40 Hours**

Detailed Syllabus

Module 1: Fundamentals of RTL Design

- Introduction to **RTL design methodologies**
- Understanding **combinational and sequential logic**
- Design flow from **RTL to GDSII**

Module 2: Verilog/VHDL Programming

- Data types, operators, and syntax rules
- Procedural and continuous assignments
- Structural and behavioral modeling
- Testbenches and debugging techniques

Module 3: RTL Coding Guidelines & Best Practices

- Writing **synthesizable RTL code**
- Avoiding **latch inference and race conditions**
- Optimizing RTL for **timing and area efficiency**

Module 4: Synthesis using Synopsys Design Compiler

- Understanding **logic synthesis process**
- Writing **Synthesis Constraints (SDC files)**
- Analyzing **reports (area, timing, and power)**
- Gate-level optimization