

## Certificate Course in VLSI Design

### Course Objective:

This course aims to providing detailed knowledge in VLSI design process starting from digital design, hardware descriptive languages, RTL, synthesis & simulation, verification, FPGA programming & implementation. In this process the student will understand the entire logic design process and will be able to take on the challenges posed by the even demanding chip design industry.

**Learning Outcomes:** After the end of the course the student will be able to complete a significant VLSI design project having a set of objective criteria and design constraints.

**Expected Job Roles:** VLSI Engineer

**Course Duration(in hours )(in hours)** : 80 hrs

**Course Fee (INR):** : Rs.12000/-(+GST as applicable)

**Minimum Eligibility** : Engineering Graduates (Undergoing also)

### Course Outline:

S.No	Topic	Minimum No of Hours
1.	Advanced Digital Design Review	12 hrs
2.	Hardware Description Language (Verilog HDL)	40 hrs
3.	FPGA Architecture and Prototyping	28 hrs
<b>Theory / Lecture Hours:</b>		30 hrs
<b>Practical Hours:</b>		50 hrs
<b>Total Hours</b>		80 hrs

**Books recommended** : Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition. By **Samir Palnitkar**

## **QUALIFICATION FILE: Certificate Course in VLSI Design (Level 05)**

### **Annexure – I** **Course Curriculum**

#### **1: Advanced Digital Design Review**

**Duration:** 12 Hours

#### **Objective**

The objective of the course is to provide understanding of the entire logic design process with the analysis from combinational and sequential digital circuit design.

#### **Course Description**

- Combinational Circuit Design
- Sequential Circuit Design
- Design of controller and Data path units
- State Machines
- Controller Design using FSMs & ASMs
- Design Examples & Case Studies

#### **Learning Outcomes**

After successful completion of the module, the students shall be able to:

- 1 Analyze combinational and sequential circuit design concepts.
- 2 Develop FSMs & ASMs for the given problems.

#### **Text Books:**

1. Modern Digital Electronics. Author, R P Jain. Edition, 3. Publisher, Tata McGraw-Hill Education
2. Wakerly, John F.. Digital Design Principles and Practices,

#### **2: Hardware Description Language (Verilog HDL)**

**Duration:** 40 Hours

#### **Objective**

## **QUALIFICATION FILE: Certificate Course in VLSI Design (Level 05)**

The objective of the course is to provide understanding of the techniques essential to the Verilog programming for Verification and Testing.

### **Course Description**

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Modeling methods.
- Design Verification using Test benches

### **Learning Outcomes**

After successful completion of the module, the students shall be able to:

- 3 Write Verilog code, compile, simulate and execute on any VLSI design platform.
- 4 Perform verification and testing

### **Reading List**

1. VHDL Programming By Example By Douglas Perry-PHI
2. Verilog HDL, 2/E By Samir Palnitkar, Pearson Education

## **3: FPGA Architecture and Prototyping**

**Duration:** 28 Hours

### **Objective**

FPGAs are the present day tool for implementing many embedded applications. A basic understanding of digital electronics is very useful for the proper understanding of this topic. Basics of communication are also covered for further applications.

The course is structured to include the learning of Verilog HDL syntax and the architecture of most prominent vendor in the FPGA market, Xilinx FPGAs and Altera FPGAs. Hands own experiments and a mini-project are included in the module.

### **Course Description**

## **QUALIFICATION FILE: Certificate Course in VLSI Design (Level 05)**

- Introduction to Programmable Logic and FPGAs
- Popular CPLD & FPGA Families
- Architecture of popular Xilinx and Altera FPGAs
- FPGA Design Flow
- Implementation Details
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Static Timing Analysis
- Design problems (Mini Project)

### **Learning Outcomes**

On completion, the participants will be able to:

- 1 Apply Verilog HDL for FPGA Programming
- 2 Implement Digital Circuits on Xilinx FPGAs and Altera FPGAs using Verilog HDL

### **Reading List**

FPGA Users Guides and Datasheets From Xilinx & Altera