C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Compare f_{max} of a 4-bit ripple counter with that of a 4-bit synchronous counter using J-K FFs. The t_{pd} for each FF is 50ns and t_{pd} for each AND gate is 20ns. What needs to be done to convert these counters to mod-32? Determine f_{max} for the mod-32 ripple and parallel counters.

b) Derive a truth table for the following expression (F) by showing each element in the truth table and minimize the function (F).

$$F = \overline{A \bullet C} \bullet (B \oplus D) + A \bullet \overline{C} \bullet \overline{(B \oplus \overline{D})} + B \bullet \overline{C} \bullet D + \overline{B + C + D}$$

c) Convert a clocked D flipflop to a clocked JK flipflop by adding external gates.

d) Find the base of the following operation:

23+44+14+32=223

e) VHDL is a concurrent language. Show its use in the design of sequential circuit.

f) Differentiate between inertial delay model and Transport delay model in terms of signal assignments.

g) Explain threshold voltage and Noise margin for CMOS inverter.

(7x4)

2.

a) Realize $F_1(a,b,c)=\Sigma m(0,2,3,4,5)$, $F_2(a,b,c)= \Sigma m(0,2,3,4,7)$, $F_3(a,b,c)= \Sigma m(1,2,6,7)$ using only 2-input NAND gates.

b) A sequential network contains a register of four flipflops. Initially a binary Number N (0000<=N<=1001) is stored in the flipflops. After a single input pulse is applied to the network, the register should contain N+0101. In other words, the function of the sequential network is to add 5 to the contents of a 4-bit register. Design the network using J-K flipflops.

c) Design a sequence generator by using JK flipflops which goes through following sequences: 0,3,5,6 and repeat. Determine whether the counter is self starting or not?

(6+6+6)

3.

a) Simplify the function using Karnaugh Graph $f(a, b, c, d) = \sum m(0, 2, 10, 11, 12, 14)$.

b) Realize the following functions using a PLA. Show all steps of design.
$F_1=\Sigma m(2,3,5,7,8,9,10,11,13,15)$
$F_2=\Sigma m(2,3,5,6,7,10,11,14,15)$
$F_3=\Sigma m(6,7,8,9,13,14,15)$

(6+12)

4.

a) Give VHDL description of a T flipflop.

b) Using developed description of the T fliplfop design a 3 bit asynchronous counter. Give VHDL description of a counter in a structural modeling style.

(9+9)

5.

a) Draw a block diagram of a 4 bit serial adder with Accumulator. Explain operation of it and also describe control state graph.

b) Explain static '1' hazard in combinational circuit by taking a suitable example.

c) Using two 2-to-1 multiplexers (with no added gates) design a 3-to-1 multiplexer. Input selection should be as follows:

Input Selection	AB
I_0	00
I_1	01
I_2	1X

(10+4+4)

6.

a) Design a 2-input 2-output synchronous sequential circuit which produces an output z=1, whenever any of the following input sequences 1100, 1010 or 1001 occurs. The circuit resets to its initial state after a 1 output has been generated.

b) Realize a 2-bit comparator to compare two 2-bit numbers, using appropriate demultiplexer with active high outputs and additional logic gates.

c) Design a hexadecimal to binary encoder using 74148 encoders and 74157 multiplexer.

(6+6+6)

7.

a) 4 unsigned 4-bit numbers are stored in a set of registers. Design a circuit that can sort the list in ascending order. Draw a possible system architecture diagram, showing different components, which are required for the design.

b) Draw and explain the basic structure of FPGA. Explain functioning of logic cell using lookup table approach.

c) Design the sequential circuit whose state table is given below using a 2-bit register and combinational gates.

Present State		Input	Next state	
A	**B**	**X**	**A**	**B**
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(8+6+4)