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Message from Secretary Ministry of Electronics & Information Technology



The Government of India has taken a number of landmark initiatives. The 'Digital India' program is committed to take the cause of good governance forward, in both letter and spirit. Digital India is viewed as a 'game changer', from the perspective of delivery of pro-citizen good governance, with the synchronized and coordinated engagement of the entire Government.

As one of the most sustainable and dependable arm of MeitY, NIELIT has endeavored to lead by example through institutionalization of policies and best practices. It has emerged as a key player in training related services. NIELIT courses are already known throughout India for its high standards of quality and these courses are also supported by an unfaltering and holistic system of examination at the nationallevel.

I am happy to note that through proactive use of technology, capacity building and process re- engineering initiatives, NIELIT has made efforts to leverage its capacity and create synergy in the area of training and support services. Also, in tune with the changing times, NIELIT has diversified and spread its wing by expanding its repertoire of activities. Recently, NIELIT has also taken up new capacity building initiatives in the areas of e-Governance, Digital Marketing, Cloud Computing, Big Data, IoT etc. e-Contents are being developed to usher in a new paradigm of learning.

I would also like to compliment NIELIT for its efforts to standardize its Short-Term Courses across all NIELIT Centres. The Student Support Services have been also upgraded with the introduction of web-based services and a Placement Portal has been institutionalized by NIELIT, which would facilitate the students to seek suitable employment. Such proactive measures are the need of the time and I am happy that NIELIT is introducing such features with the required sensitivity and vibrancy.

I congratulate NIELIT for its endeavor to spread IT literacy and education across the country. The efforts made by NIELIT in implementing various government schemes by scaling up its operations and leveraging its capacities, are praiseworthy.

The integrated NIELIT Website is a welcome step towards uniformity, dynamism and improved services for stakeholders and I wish NIELIT success in its future efforts.

(Ajay Prakash Sawhney)



Message from Director General

The National Institute of Electronics and Information Technology (NIELIT), a body under the administrative control of the Ministry of Electronics and Information Technology (MeitY), Government of India, a distinct identity and character in the panorama of Skill Development and Capacity Building in India. With presence at 42 locations across the country and a network of around 1000 Accreditation Centres, NIELIT is uniquely positioned in terms of its outreach to all corners of the country and all segments of the society.

NIELIT has made efforts to establish standards in the areas of IECT (Information, Electronics and Communication Technology) in both formal and non-formal mode of education. As the education system in this country is undergoing a paradigm shift to improve upon the employability factor, NIELIT is offering a rich repertoire of market-oriented courses in the emerging areas viz Cyber Security, IoT, ESDM, GIS, Cloud Computing, Hardware, Electronics Design Technology, VLSI Design, Embedded Systems, e-Waste, Big Data as per needs of the IT and the electronic industry.

NIELIT Aurangabad is one of the prominent centre of NIELIT that was setup in the year 1987 in order to bring an **innovative**, **entrepreneurial spirit** and to maintain close links with Industries, R&D and Academic Institutions to promote electronics, IT and industrial design culture. Owing to its quality and solution-oriented skilling approach, the centre has produced many prominent **entrepreneurs**, **experts** and **designers**.

As per the aegis of Make-in-India, the Centre is providing Quality Technical Education through **B. Tech.** (Electronics System Engineering), M. Tech. (Electronics Design and Technology) and Diploma in Electronics Production and Maintenance leading to Academic Excellence, Creativity and Innovation in the areas of IECT that helps to develop employable workforce and shape entrepreneurs. It is also a Research Centre of the Dr. Babasaheb Ambedkar Marathwada University, Aurangabad for conducting research leading to award of Ph.D. Degree in Engineering and Technology.

I am confident that by taking admission at Aurangabad centre of NIELIT, the students would be greatly benefitted by some of the best facilities in the country like Industrial R&D Infrastructure, state-of-the-art Labs, well equipped Library, NKN, rich repertoire of e-journals, Hostel, Gymnasium, Sport Facility.

(Jaideep Kumar Mishra)





The **NIELIT Aurangabad** Centre (erstwhile CEDTI) is one of the prominent Centres of NIELIT that was established in the year 1987 to bring an **innovative**, **entrepreneurial spirit** along with excellence in teaching, learning and research to develop leaders in IT and Electronics. It is co- located in Dr. Babasaheb Ambedkar Marathwada University (BAMU) campus and possesses state- of-the-art 14 well equipped laboratories and Mechanical workshop besides a rich Library, NKN, Gymnasium for students, Auditorium, Hostel, Canteen, Sports facility spread over more than 18 acres.

The Centre is offering AICTE approved B. Tech (Electronics System Engineering), M. Tech (Electronics Design and Technology), Diploma in Electronics Production & Maintenance and is also a Research Centre of the Dr. Babasaheb Ambedkar Marathwada University, Aurangabad for conducting research leading to award of Ph.D. Degree in Engineering and Technology.

Based on **project-based** teaching methodology, these courses provide practical skills in in the areas of **Electronics Design & Technology** and includes interdisciplinary field issues such as requirements engineering, industrial design, product engineering, ergonomics, aesthetics, System-level packaging, thermal design, reliability, EMI&EMC, testing & evaluation, maintainability, Serviceability necessary for successful system development, design, implementation and ultimate disposal after decommission. These courses take into account latest **industrial trends** & **requirements** and trains students to become **entrepreneurs**, **experts** & **designers**, carry out **R&D** and provide **Industrial Consultancy** in IECT.

NIELIT Aurangabad Centre is promoting Industry Oriented Projects, R & D and consultancy to raise the overall standards. The Centre reckoned on the ideology that identifying the needs of modern engineering & technology education for modern age students supplemented with a vision& mission will lead to a greater education system which is outcome oriented, transparent, accountable & accessible and is also effective in keeping ourselves abreast and keep us way ahead of our competitors.

All the faculty members and scientists working at Centre are striving hard to impart **professional education**, combined with fostering **innovative thinking**, **application of knowledge**, inculcating **professional ethics** and consciousness to social responsibilities. Our core values of excellence, integrity, transparency, quality, team work, execution with passion, trust, continuous and student centric learning are all closely integrated into our academic programs.

I encourage you to explore all that NIELIT Aurangabad Centre has to offer and I am confident that each one of you graduating from the Centre will leave your indelible mark of success in whichever sphere of life you choose to be.

Governing Council of NIELIT



Shri Ashwini Vaishnaw
Chairperson
Hon'ble Minister of Railways,
Communications and
Electronics & IT



Shri Rajeev Chandrasekhar Deputy Chairperson Hon'ble MoS Skill Development & Entrepreneurship and Electronics & IT



Shri Ajay Prakash Sawhney Executive Vice Chairperson Secretary, Ministry of Electronics and IT



Shri Amit Khare Member Secretary, Department of higher Education Ministry of Human Resources Development



Prof. Dhirendra Pal Singh Member Chairman, UGC



Prof. Anil D. Sahasrabudhe Member Chairman, AICTE



Ms. Jyoti Arora Member Additional Secretary & Financial Adviser, MEITY



Dr. Jaideep Kumar Mishra Member, DG NIELIT, Joint Secretary & Group-Coordinator



Shri Rajiv Kumar Member Joint Secretary,MEITY



Shri Rajesh Aggarwal Member, Director General (Training), DGET Ministry of Skill Development & Entrepreneurship



Mrs. Debjani Ghosh Member President, NASSCOM



Prof (Dr) J W Bakal Member President, IETE



Prof. Pushpak Bhattacharya, Member, Director, Department of Comp. Sci. & Engg., IIT Patna



Shri Hariom Rai Member Chairman, Lava International Limited



Shri. T.V. Mohandas Pai Member, Chairman Manipal Global Education Services pvt. ltd.



Shri. Vineet Nayar Member, Founder Sampark Foundation

CONTENTS

Sr. No.	Details	Page No.
	SAY NO TO RAGGING	
1.0	NIELIT Aurangabad – An Introduction	1-5
2.0	Formal Courses	6-7
3.0	DEPM	8-14
4.0	B. Tech (Electronics Engineering)	15-22
5.0	M.Tech (EDT) Full Time	23-27
6.0	M.Tech (EDT) Part time	28-32
7.0	Partial List of Teaching Staff	33-35
8.0	Placement Assistance	36
8.0	Partial List of Alumni	37-39
10.0	Refund of fees in the event of cancellation of admission	40

Annexure Details

Annexure No.	Purpose	Page No.
Annexure-I	Tentative Academic Calendar	41
Annexure-II	Assessment Computation of SGPA & CGPA	42
Annexure-III	Application form for Lateral Entry Admission (Direct 2nd Year) of 3 Years DEPM (Diploma in Electronics Production and Maintenance)	43
Annexure-IV(A)	Application Form for Eligibility cum Admission to DIPLOMA/B.Tech/M.Tech Full Time for Foreign Nationals	44-45
Annexure-IV(B)	Declaration and Undertaking for Foreign Nationals	46
Annexure-IV(C)	Declaration and Undertaking	47
Annexure-V	Application form for Lateral Entry Admission (Direct 2nd Year) of 4 Year B.Tech (Electronics System Engineering)	48
Annexure-VI	Application form for 3 Years M.Tech (Electronics Design Technology) Part Time Course Admission	49-50
Annexure-VII	SC/ST Caste Certificate (Format)	51-52
Annexure-VIII	OBC Caste Certificate (Format)	53-54
Annexure IX	Physical Disability Certificate (format)	55
Annexure X	Physical Fitness Certificate (format)	56
Annexure XI	Sponsorship Certificate	57
Annexure XII	No Objection Certificate for M.Tech (EDT) Part Time Candidate	58

SAY NO TO RAGGING

According to UGC guidelines, the definition of ragging states that any conduct whether by words spoken or written or by an act which has the effect of teasing, treating of handling with rudeness any other student, indulging in rowdy or undisciplined activities which causes or is likely to cause annoyance, hardship or psychological harm or to raise fear or apprehension thereof in a fresher or a junior student or asking the student to do any act or perform something which such student will not in the ordinary course and which has the effect of causing or generating a sense of sham or embarrassment so as to adversely affect physique or psyche of a fresher or a junior student.

IMPORTANT INSTRUCTIONS FOR THE STUDENTS

- 1. As per the directions of the Hon'ble Supreme Court in SLP No. 24295 of 2006 dated 16-05-2007 and in Civil Appeal number 887 of 2009, dated 08-05-2009, ragging is strictly prohibited and banned.
- 2. All students of the institute have to study and fill affidavit online. http://antiragging.in/site/affidavits_registration_form.aspx.
- 3. Ragging is a Cognizable Offence. Students are advised not to indulge in Ragging.
- 4. Ragging entails heavy fines and/or suspension/expulsion.
- 5. In case the applicant for admission in the institute is found to have indulged in ragging in the past or if it is noticed later that he has indulged in ragging, admission may be refused or he/she shall be expelled from the institution
- 6. It is mandatory for the parents to report immediately to the Authorities of the Institute in case their wards inform them about ragging.

PUNISHABLE INGREDIENTS OF RAGGING

- 1. Abetment to ragging or Criminal conspiracy to rag
- 2. Unlawful assembly and rioting while ragging
- 3. Public nuisance created during ragging
- 4. Violation of decency and morals through ragging
- 5. Injury to body, causing hurt or grievous hurt
- 6. Wrongful restraint or Wrongful confinement
- 7. Use of criminal force
- 8. Assault as well as sexual offences or unnatural offences
- 9. Extortion or Criminal intimidation
- 10. Criminal trespass or Offences against property
- 11. Attempts to commit any or all of the above mentioned offences against the victim(s)
- 12. Physical or psychological humiliation
- 13. All other offences following from the definition of "Ragging"

PUNISHMENT

Depending upon the nature and gravity of the offence as established by the Anti-Ragging Committee of the institution, the possible punishment for those found guilty of Ragging at the Institution level shaped any one or any combination of the following:

- 1. Suspension from attending classes and academic privileges
- 2. Withholding/Withdrawing scholarship/fellowship and other benefits
- 3. Debarring from appearing in any test/ examination or other evaluation process
- 4. Withholding results
- 5. Debarring from representing the institution in any regional, national or international meet, tournament, youth festival etc.
- 6. Suspension expulsion from the hostel
- 7. Rustication from the institution for period ranging from 1 to 4 semesters
- 8. Expulsion from the institution and consequent debarring from admission to any other institution for a specified period
- 9. Fine ranging between Rupees 25,000/- and Rupees 1 Lakh
- 10. Collective punishment: When the persons committing or abetting the crime of ragging are not identified, the institution shall resort to collective punishment
- 11. Fresher who do not report the incidents of ragging either as victims or as witnesses shall also be punished suitably.

As per the directions of the Hon'ble Supreme Court of India, if any incident of ragging comes to the notice of authority, the concerned student shall be given liberty to explain and if his/her explanation is not found satisfactory, the authority would expel him/her from the Institute"

1.0 NIELIT Aurangabad -An Introduction

1.1 Genesis

The history of NIELIT dates back to 1974 when the Department of Electronics (DoE) now Ministry of Electronics and Information Technology (MeitY), Govt. of India and the University Grants Commission (UGC) set up the first CEDT within the premises of **Indian Institute of Science (IISc.)**, **Bangalore** with assistance from Swiss Development Corporation.

A decade after the successful running of CEDT, Bangalore, DoE (now MeitY) set up similar centres at Aurangabad, Imphal and Srinagar in 1987, Calicut, Mohali and Gorakhpur in 1989, with an objective to develop human resources at different levels and in different specialized areas of Electronics Design. Aim was to bridge the gap between the academic institutions and industries.

The CEDT centres based at Aurangabad, Calicut, Gorakhpur, Imphal and Srinagar were merged with **DOEACC** (a scientific society of MeitY) in 2001. In order for its metamorphism into an **Institute of National Importance** the Society was renamed as 'National Institute of Electronics and Information Technology (NIELIT) on October 10,2011.

The **NIELIT Aurangabad** is co-located inside the lush green campus of Dr. B.A.M. University and its campus is spreads over **more than 18 acres**. It has about **14 well equipped laboratories** and **Mechanical workshop** besides a rich Library, Gymnasium for students, Auditorium, Canteen, Basket-ball ground, Volley ball ground, Kho Kho ground etc.

The Centre started offering unique AICTE approved courses viz **Diploma in Electronics Production and Maintenance** since 1987, **M.Tech (Electronics Design and Technology)** since 1990, **B Tech (Electronics System Engineering)** since 2013 and is also a Recognized Research Centre of the Dr. B.A.M. University, Aurangabad since 2007 for conducting research leading to award of Ph.D. Degree in Engineering and Technology.



The Centre also provides **consultancy** and other services to leading **Industries** of the region like Bajaj Auto Ltd, Videocon, Sterlite, Siemens, Meltron, Maharashtra Police Wireless, etc. It is also implementing **ESDM scheme** sponsored by **Ministry of Electronics and Information Technology** (**MeitY**) for developing human resource with adequate competence levels in **Electronics Design & Production Technologies.**

The Industrial grade laboratories of the Centre are fully equipped with the latest systems and development tools in the area of Printed Circuit board, VLSI Design, Embedded Systems, Product Design, Digital Systems, Process Control & Instrumentation and in CAD/CAM.

Besides numerous reference books, Journals, magazines; the students of the Centre have access to **MeitY Library Consortium** (rich collection of latest e-Journals including IEEE and books) and **National Knowledge Network** (**NKN**) a strong a network with multi-gigabit capability connected to all universities, research institutions, libraries, laboratories, healthcare and agricultural institutions across the country.

All the labs, library and office are connected through the central network and students can retrieve information from their terminals itself and through well connected Wi-Fi system. The Centre organizes **National Level Seminars/Workshops** in areas like Agri- Electronics, Electronics Product Design, Intellectual Property Rights (IPR), Neural Networks, e-learning regularly.

Trained to become R&D engineers students of the centre are working in **leading and reputed organizations** like C.G Coral. Lucent India, Texas, L&T, HCL, Wipro Technologies, BITS, IIT, BEL, HAL, ISRO, DRDO, BARC, ECIL, Messung, Thermax, Honeywell Cyrus logic L&T EMSYS to name a few.





The Centre has become a solution-oriented model organization and knowledge-based enterprise and is tirelessly working for creating a pool of R&D engineers and Entrepreneurs.

1.2 Objectives of Centre

- 1. To bring an **innovative**, **entrepreneurial spirit** along with excellence in teaching, learning and research to develop leaders in IT and Electronics.
- 2. To generate and keep update **Industry-ready quality professionals** with **knowledge-based skill set** in IECT and allied fields through formal and informal education system.
- 3. To establish a **Quality system of examination and certification** that is globally recognized and provides a fair assessment of the competency of students.
- 4. To maintain **close links** with **Industries**, **R&D** and **Academic Institutions** to promote electronics, IT and industrial design culture.
- 5. To develop entrepreneurs, experts and designers, carry out R&D and provide
- 6. **Industrial Consultancy** in IECT.
- 7. To offer **e-Training** in Electronics, Information Technology and Industrial Design methodology and production technique.

<u>Mission:</u> Identifying the needs of modern engineering & technology education and providing Quality Technical Education leading to Academic Excellence, creativity and innovation in the areas of Electronics and Information Technology.

<u>Vision:</u> To impart professional education that is outcome oriented, combined with fostering innovative thinking, application of knowledge, inculcating professional ethics and consciousness to social responsibilities.

1.3 Product Design

The Centre is providing world-class educational & skill development opportunities to the youth and the course structure at the Centre is designed to inculcate system level understanding among the students. Most of the M.Tech. Projects are sponsored by companies and result in Hardware Electronic Products. Some of the students later transform their knowledge into commercial ventures.





Industry Interaction:

The institute also provides services like product design & development, product engineering, proto-type development, process automation, consultancy, etc.to industries. The institute is also making all efforts to create best infrastructure to provide quality services to industry in servicing and maintenance of sophisticated instruments / machines, support in technology absorption and procurement of latest equipment/ machines.

1.3 R & D, Projects and Consultancy

Post Graduate level academic projects are of one (01) year duration, whereas Diploma and B.Tech level projects are of one (01) semester (six months) duration. Students are encouraged to interact with industry to expose them to industry environment and motivated to undertake real problems of industry as their innovative project work, guided by the faculty. In addition to above, the institute also undertakes Government as well as industry sponsored projects. Some of them are "Training of Teachers in e-learning", "Information Security Education & Awareness" and Women Empowerment through Value Added Skill Development in IECT". Apart from above, the consultancy is also provided to the industry.

1.4 Some of the laboratories

- i. CAD/CAM
- ii. Consumer Electronics
- iii. Industrial Automation
- iv. Internet of Things
- v. Network & Server Facilities
- vi. Opto-Electronics
- vii. Power Electronics
- viii. Printed Circuit Board
- ix. VLSI Design
- x. Embedded System Design
- xi. Open-Source Computing
- xii. AR/VR Lab
- xiii. Library Infrastructure
- xiv. Multimedia Lab
- xv. Additive Manufacturing/3D Printing Lab

1.5 Other Amenities /Facilities:

Lecture Halls	Uninterrupted Power (63
	KVA DG Set)
Seminar Hall	Cafeteria
Conference Hall	Boy's Hostel
Auditorium	PG Boy's Hostel
Local Area Network with 225 (100 Mbps) Nodes.	Warden Quarters
Leased line internet connectivity	Guest House
Library with online access to IEEE Journals and National Digital Library	Vehicle Parking
of India along with a rich print collection of books, journals and magazines	
(refer Annexure XXVI)	
Virtual Smart Class-Room facility	Open Theatre
Placement Cell and Model Career Centre	Record Room (143 Sqm)
Gymnasiums(Separate for Boys & Girls)	Sports Facilities
Dramatics, dance and Extra-Curricular	Jogging Track

1.6 Student Life

The course work is project based and students get ample time to work on innovation. There are various sports and cultural clubs that are being managed by the student community on campus which serve for various extra-curricularactivities:

- 1. Cricket
- 2. Badminton
- 3. Lawn Tennis
- 4. Basket-Ball
- 5. BodyBuilding
- 6. Drama Club
- 7. MusicClub
- 8. Athletics
- 9. Literary and FineArts
- 10. Photography





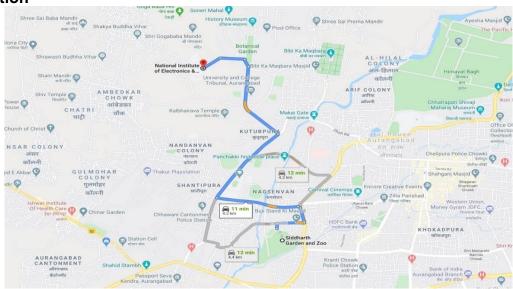








1.7 Location



NIELIT Aurangabad

Dr. Babasaheb Ambedkar Marathwada University Campus,

Aurangabad, Maharashtra-431004

Website: http://nielit.gov.in/aurangabad/ Landline:(+91-240) 2982021,2982022 Telephone/Fax: (+91-240) 2982050

2.0 Formal Courses

The Institute is offering following AICTE approved courses:

- A) Diploma in Electronics Production and Maintenance (DEPM)
- B) B. Tech in Electronics System Engineering.
- C) M.Tech in Electronics Design and Technology
- D) Part-time M. Tech in Electronics Design and Technology

These courses are practical oriented and are designed with an emphasis on design and project work. The quality of education is maintained by periodic review and update of syllabus considering the latest trends and needs of industry, in-depth study by the students through semester system, transparent evaluation system and flexibility being autonomy granted to the Centre by Dr. B.A.M. University, Aurangabad(M.S). The Centre enjoys the reputation of its students getting employed in reputed industries and organizations almost immediately on their completion of courses or settled as successful entrepreneur.

Important Dates

Sr.	Last date	DEPM	DEPM	B.Tech	M.Tech	M.Tech
No.	555 \$-555	First	(Lateral	(Lateral	(EDT) Full-	(EDT)
		Year	Entry)	Entry)	time	Part-time
1.	Downloading Application form from website		14 th August, 2021	14 th Augus t, 2021		14 th August, 2021
2.	Receipt of Application Form along with Fees	Plea se	10 th Sept, 2021	10 th Sept, 2021		10 th Sept, 2021
3.	Written Test (tentative)	visit - web site -	13 th Sept, 2021	13 th Sept, 2021		13 th Sept, 2021
4.	Declaration of list of selected & waitlisted Candidates	@ ww w.dt	15 th Sept, 2021	15 th Sept, 2021	Please visit website www.ccmt.ni	15 th Sept, 2021
5.	Document Verification and Admission to the course	ema hara shtra .gov.	15 th Sept, 2021	15 th Sept, 2021	c.in	15 th Sept, 2021
6.	Waitlist student Admission	in	17 th Sept, 2021	17 th Sept, 2021		17 th Sept, 2021
7.	Academic calendarstarts		1 st Oct. 2021	1 st Oct. 2021		1 st Oct. 2021

^{**} All the dates are tentative and any change in date will be displayed on the website only

Important Links

	tuit Lims	
Sr.No	Purpose	URL
1.	Downloading of Application Form	https://www.nielit.gov.in/aurangabad
2.	List of Selected & Waitlisted Candidates	
3.	Date and time for operation of the waiting list	

^{**} List of Selected & Waitlisted Candidates will be displayed on the website only

^{**}The dates for admission in Diploma course will be as per the schedule of CAP 2021.

^{**} The dates for admission in B.Tech course will be as per the schedule of JoSSA/CSAB 2021

^{**} The dates for admission in M. Tech course will be as per the schedule of CCMT 2021

^{**} The Competent Authority at his discretion may extend the Last date

Process for Payment for Fees

Name of the	National Institute of Electronics and Information Technology
Institute/Beneficiary	(NIELIT)
Name of the Bank	State Bank of India
Branch	Samarth Nagar Aurangabad Maharashtra
Saving Bank Account Number	32078399585
IFSC/RTGS NO	SBIN 0007919
Mode of Electronic Transfer	NEFT, SBICollect, Website: www.onlinesbi.com

Syllabus of Written test

Sr.	Purpose	Syllabus	Subjects
no			
1.	DEPM (Direct)	X standard of CBSE	Science, Mathematics & English
		Board	
2.	DEPM(Lateral Entry)	XII standard of CBSE	Physics, Chemistry and Mathematics
	-	Board	& English
3.	B.Tech (Lateral Entry)	Diploma (Electronics)	recognized by State/Central Board of
		Technical Education	
4.	M.Tech (EDT) for part	Gate 2021 Syllabus for	(Common Subject of Electronics and
	time	Communication/Instrumer	ntation Engg. /Electrical Engg)

Written Test for Admission

- 1. The written entrance test will be of 1½hours duration
- 2. The question be of objective type, wherein the candidate is provided, multiple choice answers
- 3. The candidate is required to mark the correct answer in the same sheet, provided to him/her.
- 4. The candidates are required to bring Pen, HB Pencil, Sharpener and Eraser.
- 5. Candidates are not allowed to take the Question/Answer booklet outside the exam hall.
- 6. Test will be in English Medium only.
- 7. Calculators, Mobile, Digital Diary, Log books and Pocket PCs are not allowed in the Exam Hall.
- 8. Conduction of written test is subjected to the number of candidates applied for the course.

Important Information

- 1. The student is required to submit the undertaking to agree to abide by the terms and conditions of the institute and AICTE New Delhi at the time of admission in the prescribed format as per Annexure V(C) and counter signed by parent / guardian.
- 2. The students are encouraged to interact with industry for getting familiar to industry environment and to study & undertake real problems being faced by them as their project work.
- 3. All the students (boarders as well as day scholars) are required to strictly abide by the rules of the Institute / Centre, failing which disciplinary action may be taken against them.
- 4. The mess is attached to the hostel.
- 5. Mess–Canteen facility is compulsory for the students who reside in NIELIT Hostel.

3.0 Diploma in Electronics Production & Maintenance (DEPM)

This is a three- year (Six Semesters) course, which grooms students for a career as Production/Maintenance Supervisor or Design Assistant in Electronics or allied industry or entrepreneur. The course is approved by AICTE, New Delhi and Maharashtra state Board of Technical Education (MSBTE), Maharashtra (India).

3.1 Admission in 1st Year

3.1.1 Minimum Eligibility Criteria

Xth **standard/Secondary School Certificate** (**SSC**) Examination passed from a recognized Board with a minimum average score of 35% in Mathematics and Science subjects.

3.1.2 Seat Matrix

Sr. No.	Course Name	Total
1	Diploma Electronics Production & Maintenance (DEPM)	60*

^{*}Number of seats indicated above are tentative and subjected to be change by Government orders given time to time.

Important

- i. Seats are reserved for candidates belonging to reserved categories as per Government of India Rules and approval of AICTE, New Delhi.
- ii. General, OBC, SC, ST, PWD and Foreign National Seats are reserved as per Govt. of India Rules, AICTE and/or University Approval.
- iii. Seats for Foreign Nationals are reserved as per Government of India Rules and University approval.

3.2 Lateral Entry/Direct Admission in 2nd Year

3.2.1 Minimum Eligibility Criteria

XII standard/ Higher Secondary Certificate (HSC) Examination passed from a recognized Board with Physics, Chemistry and Mathematics

 \cap R

ITI (Electrical / Electronics) from recognized Institute.

3.2.2 Seat Matrix

12 Seats + Vacant Seats (if any)

Note: General, OBC, SC, ST, PWD and Foreign National Seats are reserved as per Govt. of India Rules, AICTE and/or University Approval.

3.3 Selection Process

(A) National Applicants

- i. Only the Candidates meeting the minimum eligibility criteria will be eligible for admission.
- ii. Admission to DEPM program for 1st year will be through centralized Admission Process (CAP) conducted by DTE Maharashtra, Visit the official website of the Directorate of Technical Education, Maharashtra @ www.dtemaharashtra.gov.in.
- iii. The Merit List for Lateral Entry in 2nd Year to DEPM program will be based on the score in the Written Test and/or score in XII standard/ Higher Secondary Certificate (HSC)/ ITI (Electrical)/ ITI (Electronics) Examination.

- iv. Admission of the Selected Candidates will be subject to their verification of Documents and payment of applicable fees.
- v. The category-wise Main List (selected) and Waiting List of the candidates for admission to (year 2021-22) of DEPM Course will be displayed on the website and Notice Board of the Institute.
- vi. The date and time for operation of the waiting list shall also be declared along with the list of selected candidates. All the waitlisted candidates should make themselves available at the time of counselling of the waiting list, otherwise their claim shall be forfeited.
- vii. The waitlisted candidates, available at the time of counselling of the waiting list, shall be provisionally admitted as per the merit of the category-wise waiting list.
- viii. The selected main and waiting list candidates are required to register on the day as notified along with the list of documents asked and by making payment as mentioned in **Section 3.13** for admission in 1styear and **Section 3.14** for Lateral Entry/Direct Admission in 2nd Year, otherwise their claim shall be forfeited.
- ix. Admission process of the DEPM Course is completed when the approved intake of candidates as per Seat Matrix are provisionally admitted and registered or a time limit decided by the competent authority is over, which- ever is earlier.

B) International Applicants for admission for 1st year

- i. Admission of Foreign Nationals is subject to guidelines, laid down by Government of India from time to time.
- ii. Persons of Indian Origin (PIO) is an individual with foreign citizenship, except Pakistan and Bangladesh, without "NRI" status, holding a Foreign Passport at the time of applying for admission as well as during the study period and is himself/herself or anyone/both of his/her parents or anyone/both of his/her grandparents is/was/were Indian citizens.
- iii. Children of Indian workers in the Gulf Countries (CIWG) are children of an Indian who is working in Gulf Countries under relevant working visa.
- iv. Non-Resident Indian (NRI) Candidate is Child/ward of the person having 'NRI status as defined under section 6 of the Income Tax Act.
- v. Their application, will however, be considered separately on first cum first serve basis as per the procedure, mentioned in ANNEXURE-IV(A)
- vi. Foreign nationals are required to download and submit the application form for eligibility cum admission (ANNEXURE-IV(A)) and declaration & undertaking format (ANNEXURE-IV(B)) along with payment of Rs.5000/- or equivalent foreign currency(non-refundable).

3.4 Cancellation of Secured Admissions

If any vacancy arises after completion of admission process, the vacancy may be filled on case-to-case basis at the discretion of the Competent Authority as per the following procedure:

- i. Preference shall be given as per the ranking in common merit list.
- ii. The Selected Students as per ranking in Merit List, who could not reach the Centre for admission on the pre-intimated day because of legal and/or genuine reason(s) and approaching/contacting the institute are first considered for filling the said vacancy.
- iii. After (i) & (ii), the candidates, who have not been offered the admission and approaching, may be considered.

3.5 Academic Calendar – Refer ANNEXURE –I

3.6 Scheme of Instruction for First Year:

Every student has to register for all the subjects of a Semester as mentioned below. A six weeks mandatory vocational training is arranged for DEPM students during the summer vacation at the end of IV Semester.

Semester I

G.	Course Title	Abbre	Sub. code	Teaching Scheme			G 124	Theory		Practical		Grand
Sr. No		viation		L	Т	P	Credit (L+T+P)	Total (ESE and PA)		Total (ESE and PA)		Total
								Max	Min	Max	Min	
1	English	ENG	21D11	3	1	2	5	100	40	50	20	150
2	Mathematics-I	MAT1	21D12	4	2	-	6	100	40	-	-	100
3	Physics	PHY	21D13	2	-	2	4	50	20	50	20	100
4	Chemistry	CHE	21D14	2	-	-	2	50	20			50
5	Fundamentals of ICT	ICT	21D15	2	-	2	4	-	-	50	20	50
6	Engineering Drawing	EDW	21D16	2	1	4	6	1	-	100	40	100
7	Workshop Technology	WT	21D17	-	1	4	4	1	-	100	40	100
8	Environmental Studies	EST	21D18	3	1	-	3	100	40	-1-		100
	Tota	1		18	2	14	34	400	-	350		750

Semester II

Sr.		Abbre	Sub.	Teaching Scheme			Credit	Theory		Practical		Grand Total
No	Course Title	viation	code	L	L T		(L+T+P)	Total (ESE and PA)		Total (ESE and PA)		
								Max	Min	Max	Min	
1	Mathematics-II	MAT2	21D21	4	2	-	6	100	40			100
2	Electrical Technology-I	ET1	21D22	4	-	2	6	100	40	50	20	150
3	Analog Electronics-I	ADC1	21D23	4	-	4	8	100	40	50	20	150
4	Material Technology	MTE	21D24	3	-	-	3	100	40			100
5	Computer Programming	CPR	21D25	4	-	4	8	100	40	50	20	150
6	Business Communication	ВСО	21D26	-	-	2	2	-	1	50	20	50
	Total			19	2	12	33	500		200		700

Semester III

Sr.		Abbre	Sub.	Teaching Scheme			Credit	Theory		Practical		Grand Total
No	Course Title	viation Sub.		L	Т	P	(L+T+P)	Total (ESE and PA)		Total (ESE and PA)		
								Max	Min	Max	Min	
1	Digital electronics	DET	21D31	4	-	2	6	100	40	50	20	150
2	Analog electronics-II	AE2	21D32	4	1	4	8	100	40	50	20	150
3	Electrical Technology-II	ET2	21D33	3	2	2	7	100	40	50	20	150
4	Test and Measurement	TM	21D34	4	1	4	8	100	40	50	20	150
5	Principles of Electronics Communication	PEC	21D35	4	1	2	6	100	40	50	20	150
	Total	l		19	2	14	35	500		250		750

Semester IV

Sr.		Abbre	Sub.	Teaching Scheme			Cre dit	The	Theory		Practical	
No	Course Title	viation	code	L	Т	P	(L+ T+P		(ESE PA)	Total and	PA)	
)	Max	Min	Max	Min	
1	Linear Integrated Circuit	LIC	21D41	4	-	2	6	100	40	50	20	150
2	Consumer Electronics	CEL	21D42	3	-	2	5	100	40	50	20	150
3	Microcontroller and Applications	MIC	21D43	4	-	2	6	100	40	50	20	150
4	Power Electronics	PEL	21D44	3	-	2	5	100	40	50	20	150
5	Digital Communication Systems	DCS	21D45	4	ı	4	8	100	40	50	20	150
6	Maintenance of Electronics Equipment and EDA tool Practices	MEDA	21D46	-	-	4	4	-	-	50	20	50
	Total		•	18	0	16	34	500		300		800

Semester V

G.		A 1. 1	C I		eachi chem	0	Credit	Th	eory	Practical		Grand Total
Sr. No	Course Title	Abbre viation	Sub. code	L	Т	P	(L+T+ P)		l (ESE l PA)		(ESE PA)	
								Max	Min	Max	Min	
1	Product Design	PDE	21D51	3	-	2	5	100	40	50	20	150
2	Control system and PLC	CSP	21D52	4	ı	2	6	100	40	50	20	150
3	Embedded Systems	ESY	21D53	3	•	2	5	100	40	50	20	150
4	Mobile and Wireless Communication	MWC	21D54	4	-	2	6	100	40	50	20	150
	Elective											
5	Industrial Automation	IAU	21D55	3	-	2	5	100	40	50	20	150
	Principle of Industrial IoT	IOT	21D56	3	ı	2	5	100	40	50	20	150
6	Printed Circuit Board-I	PCB1	21D57	3	ı	2	5	100	40	50	20	150
7	Industrial Training	INTR	21D58	-	ı	6	6	1	-	50	20	50
8	8 Capstone Project planning CPP 21D59					-	3	1	-	50	20	50
	Total				0	18	41	600	-	400	-	1000

Semester VI

Sr.		Abbre	Sub.		achi chen	0	Credi	The	eory	Prac	tical	Grand Total
No	Course Title	viation	code	L	L T		(L+T +P)	Total (ESE and PA)		Total (ESE and PA)		
							11)	Max	Min	Max	Min	
1	Costing and Management	CMG	21D61	3	ı	0	3	100	40	-	-	100
2	Computer networking and Data Communication	CND	21D62	3	1	2	5	100	40	50	20	150
3	Emerging Trends in Electronics	ETE	21D63	3	-	0	3	100	40	-	-	100
4	Printed Circuit Board-II	PCB2	21D64	3	1	2	5	100	40	50	20	150
	Elective											
5	Mechatronics	MEC	21D65	3	-	2	5	100	40	50	20	150
	Optical Networks and Satellite communication	OSC	21D66	3	-	2	5	100	40	50	20	150
6	Entrepreneurship development	EDE	21D67	2	ı	2	4	-	-	100	40	100
7	Capstone Project execution and Report writing	СРЕ	21D68	-	- 1	4	4	-	-	100	40	100
8	8 VLSI with VHDL VWV 21D69				1	2	4	-	-	50	20	50
	Total				0	14	33	500	-	400	-	900

3.7 Scheme of Instruction for Direct Second Year:

Every student has to register for all the subjects of a Semester as mentioned below. A four weeks mandatory vocational training is arranged for DEPM students during the summer vacation at the end of IV Semester.

Semester III

Sr. No.	Code	Subject	Lecture	Tutorial	Practical	Credit	Marks
1.	D301	Mathematics III	3	0	0	3	75
2.	D302	Electrical Technology II	3	0	3	3	75
3.	D303	Workshop Technology	2	0	0	2	50
4.	D304	Analog & Digital	3	0	3	4	100
5.	D305	PCB Technology I	2	0	6	4	100
6.	D306	Test & Measurement I	3	0	3	4	100
7	D307	Computer &Data	3	0	6	4	100

Semester IV

Sr. No.	Code	Subject	Lecture	Tutorial	Practical	Credit	Marks
1.	D401	Analog & Digital	3	0	6	4	100
2.	D402	PCB Technology II	2	0	6	4	100
3.	D403	Test & Measurement II	3	0	3	4	100
4.	D404	Components &	3	0	0	3	75
5.	D405	Consumer Electronics	3	0	6	4	100
6.	D406	Computer &Data	3	0	6	4	100

Semester V

Sr. No.	Code	Subject	Lecture	Tutorial	Practical	Credit	Marks
1.	D501	Test & Measurement III	3	0	3	4	100
2.	D502	Power Electronics II	3	0	6	4	100
3.	D503	Microprocessors	3	0	6	4	100
4.	D504	Product Design	3	0	3	4	100
5.	D505	Material Technology	3	0	0	3	75
6	D506	Costing & Management	2	0	0	2	50

Semester VI

Sr. No.	Code	Subject	Lecture	Tutorial	Practical	Credit	Marks
1.	D601	Microcontroller	3	0	6	4	100
2.	D602	Maintenance &	2	0	6	4	100
3.	D603	Project	0	0	0	10	250

3.8 Term Course Load:

- i. In each semester, subject load varies from 18 to 41 credits per semester.
- ii. During the course period, student has to pass certain number of subjects and complete satisfactorily the assigned project work of 10 (ten) credits in the sixth semester.
- iii. On valid grounds, the authority may advise a student, who is unable to complete the course requirements in the normal period, to continue for an extra term
- iv. Diploma should be completed within six semesters.

3.9 Assessment:

i. The overall performance of a student is evaluated by assigning equal weightage to all the six semesters in order to maintain the quality of education.

- ii. A student is permitted to appear for the semester examination subject to he or she has a minimum attendance of 75% in theory and practical classes, completes all his/her sessional assignments and clears all his/her dues.
- iii. Non-appearance in any examination is treated as the student having secured zero mark in that subject examination.
- iv. The evaluation is based on an average weightage system. Every subject has credit points based on the hours of study required.
- v. Every student is assessed in a subject with equal weightage to sessional work and semester examination, thereby making the students study regularly.
- vi. Every student is awarded Grade points out of maximum 10 points in each subject. (Based on 10 Points Scale).
- vii. Based on the Grade points obtained in each subject, Semester Grade Point Average (SGPA) and then Cumulative Grade Point Average (CGPA) are computed as per **ANNEXURE-II.**

3.10 Award of Diploma:

- i. A student must complete the minimum requirement of credits in maximum period of six (6) years and must obtain a minimum CGPA of 3.3 in the course to qualify for award of Diploma.
- ii. The Diploma is awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad.
- iii. It is also recognized by Directorate of Technical Education, Government of Maharashtra.

3.11Scholarship

The Institute encourages and provides assistance to all the students, particularly the reserved category, to apply for the Central / State Govt. scholarship for reimbursement of tuition fee and maintenance allowance as per State Govt. rules.

3.12 Assistance in Placement / Pursuing Higher Studies:

The Placement Cell of the Centre offers all assistance to the students for employment / self-employment. Most of the students passing out from the Centre have good opportunities to build their career.

3.13 DEPM Fee-Structure for 1Styear admission for Academic year (2021-22)

	DEINIFEC-Structure for 1 year aumi	J							
Sr.	Particulars	1 st Sem Fees (Rs.)	2 nd Sem Fees (Rs.)						
No.		2 2011 2 003 (2133)							
1	Tuition Fee	21000	21000						
2	Caution Money Deposit*	1250							
3	Sub total	22250	21000						
	Boy's Hoste	l Accommodation							
4	Hostel Fee per Semester (5 months)	9100	9100						
5	Hostel Deposit*	2500	-1						
6	Sub total	11600	9100						
Othe	er Fees								
	Particulars	Fees							
7	Exam Fee 100.00/- per subject/ Practical								
8	Backlog Exam Fee per subject 300.00/ per subject/practical								
. ~									

^{*}Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

Important:

- i. Presently, SC/ST students are exempted from paying Tuition Fee under SP/TSP Scheme, only Caution Money deposit, hostel fee and deposit is required to be paid
- ii. Back log Exam Fee is applicable to all students appearing Backlog Exams.
- iii. Thereshallbeanincreaseupto10%in (Sl.No.1&3) in every academic year.

3.14 DEPM Lateral Entry Fee-Structure for Academic year (2021-22)

Sr. No.	Particulars	1st Sem Fees (Rs.)	2nd Sem Fees (Rs.)				
1	Tuition Fee	21000	21000				
2	Caution Money Deposit*	1250					
3	Sub total	22250	22000				
	Boy's Hostel	Accommodation					
4	Hostel Fee per Semester (5 months)	9100	9100				
5	Hostel Deposit*	2500					
	Sub total	11600	9100				
	Oth	er Fees					
	Particulars	Fees					
6	Exam Fee	100.00/- per subject/ Practical					
7	Backlog Exam Fee per subject	300.00/ per subject/practical					

^{*} Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

Important:

- i. SC/ST students are exempted from Tuition Fee (SP/TSP Scheme), only Caution Money deposit and hostel fee and deposit is to be paid.
- ii. Backlog Exam Fee is applicable to all students appearing Backlog Exams.
- iii. There shall be an increase upto 10% (SR.No.1&3) in every academic year.





^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

4.0 B.Tech.(Electronics System Engineering)

This is four years (Eight Semesters) course approved by AICTE, New Delhi. This course is designed to produces Qualified and skilled engineers capable of doing Innovative Design and Development of Electronic Products. The prospective Engineers are groomed to adopt to changing professional and societal needs through the project-oriented teaching approach. They will become qualified to work in multiple sectors viz Public Sector, Telecom Industry, IT, Automation & Instrumentation Industries.

4.1 Eligibility for Admission in 1st Year

Admission to B.Tech.(Electronics System Engineering) being offered by NIELIT Aurangabad will be made on the basis of JEE (Main) conducted by National Testing Academy (NTA)on behalf of the Govt. of India. The Joint Seat Allocation (JoSAA) / Central Seat Allocation Board (CSAB) will conduct centralized admissions for this course. For further details candidate are advised to **please visit** http://josaa.nic.in/and/ http://josaa.nic.in/

About Joint Seat Allocation Authority (JoSAA)

The **Joint Seat Allocation Authority** (**JoSAA**) has been set up by the Ministry of Human Resources Development (MHRD) to manage and regulate the joint seat allocation for admissions to IITs, ISM, NITs, IIITs and Other-Government Funded Technical Institutes (Other-GFTIs). Admission to all the academic programs offered by these Institutes will be made through a single platform.

- a. The Eligible candidate has to register and fill choices for academic program under JoSAA.
- b. Document verification will be done for acceptance of and admitting to Institute of the candidates selected by JoSAA.
- c. Special vacant seat filling round (Special round) will be conducted by Central Seat Allocation Board. For further details please visit :http://csab.nic.in
- d. The allotted candidate to NIELIT Aurangabad should report to this Institute along with the all-original certificates & Xerox copy of each documents which the candidate had verified at the reporting center in the stipulated duration and time.
- e. The candidate has to deposit the difference amount (if any) through NEFT/RTGS
- f. The fee structure is given in **Section 4.12**.

4.1.1 Seat Matrix

General	OBC	SC	ST	PW	D	Student Studying Abroad	Total
				General	OBC		
28	15	09	05	02	01	9	69

There is a separate quota of 9 seats for Student studying abroad. The interested candidates will have to take admission through DASA (https://www.dasanit.org/).

4.2 Lateral Entry (Direct Second Year) in B.Tech.(Electronics System Engineering)

4.2.1 Minimum Eligibility Criteria

Three Year Diploma in Electronics & allied streams with **minimum 45% marks** (40 percent for SC/ST candidates) are eligible for **Lateral Entry** (**Direct Second Year**) in **B.Tech**.

4.2.2 Seat Matrix

Vacant Seats (ifany)

Note: General, OBC, SC, ST and PWD are reserved as per Govt. of India Rules, AICTE and/or University Approval.

4.2.3 Selection Process for Lateral Entry

- i. Only the Candidates meeting the minimum eligibility criteria will be eligible for admission.
- ii. Admission to lateral entry (direct second year) in B.Tech will be through Maharashtra Admission regulating Authority/ written exam conducted by NIELIT Aurangabad.
- iii. The eligible candidates have to download the Application Form online and has to submit the same on **email id :btech-abad@nielit.gov.in**
- iv. The Application fees will be Rs.500/- non-refundable. However, the candidates belonging to SC/ST/PWD are exempted from application fees.
- v. The Merit List for admission to 2nd Year B.Tech (Lateral Entry) will be based on the score in the Written Test and/or score in Diploma Electrical/Electronics and allied streams.
- vi. Admission of the Selected Candidates will be subject to their verification of Documents and payment of applicable fees.
- vii. The category-wise Main List (selected) and Waiting List of the candidates for admission to (year 2021-22) of 2nd Year B.Tech (Lateral Entry) will be displayed only on the website and Notice Board of the Institute.
- viii. The date and time for counselling of the waiting list shall also be declared along with the list of selected candidates. All the waitlisted candidates should make themselves available at the time of the waiting list counselling, otherwise their claim shall be forfeited.
- ix. The waitlisted candidates, available at the time of the waiting list counselling, shall be provisionally admitted as per the merit of the category-wise waiting list.
- x. The selected candidate from main list and waiting list candidates are required to register on the day as notified along with the documents and by making payment as mentioned in Section 4.12 for admission in 1Styear and Section 4.13 for Lateral Entry/Direct Admission in 2nd Year, otherwise their claim shall be forfeited.
- xi. Admission process of the 2nd Year B.Tech (Lateral Entry) is completed when the approved intake of candidates as per Seat Matrix are provisionally admitted and registered or a time limit decided by the competent authority, which-ever is earlier.

4.3 Admission in the event of cancellation of secured admission

If any vacancy arises after completion of admission process, the vacancy may be filled on case to case basis at the discretion of the Competent Authority as per below mentioned procedure:

- i. Preference shall be given as per the ranking in common merit list.
- ii. The Selected Students as per ranking in Merit List, who could not reach the Centre for admission on the pre-intimated day because of legal and/ or genuine reason(s) and approaching/contacting the Institute are first considered for filling the said vacancy.
- iii. After (i) & (ii), the candidates, who have not been offered the admission and approaching, may be considered.

4.4 Academic Calendar – Refer ANNEXURE –I

4.5 Scheme of Instruction for First Year (2021-2022):

Every student has to register for all the subjects of a Semester as mentioned below.

Semester I

C		Cb		Feachi Schem	_	C 3:4	Theory Total (ESE and PA) Max Min 100 40 50 20 100 40	Practical		Grand	
Sr. No	Course Title	Sub. code	L	Т	P	Credit (L+T+P)		-	Total (ESE and PA)		Total
							Max	Min	Max	Min	
1	Engineering Physics	1LP01	3	1	2	5	100	40	50	20	150
2	Engineering Drawing-I	1LP02	2	-	3	5	50	20	100	40	150
3	Engineering Mathematics-I	1L03	3	2	-	5	100	40	-	-	100
4	Electrical Engineering	1LP04	3	-	2	5	100	40	50	20	150
5	Basic computer	1LP05	3	1	2	6	100	40	50	20	150

	programming, data structure and algorithm										
6	Energy and Environment Engineering	1L06	3	1	-	4	100	40	-	-	100
	Total			4	8	30	550	-	250	-	800

Semester II

		6.1		Teachi Schem	0	G P	The	ory	Pract	ical	G 1
Sr. No	Course Title	Sub. code	L	Т	P	Credit (L+T+P)	Total (ESE and PA)		Total (ESE and PA)		Grand Total
							Max	Max Min		Min	
1	Engineering mathematics-II	2L07	3	2	-	5	100	40	-	-	100
2	Engineering chemistry	2L08	3	2	-	5	100	40	-	-	100
3	Engineering mechanics	2LP09	3	-	2	5	100	40	50	20	150
4	Electronic devices	2LP10	3	-	2	5	100	40	50	20	150
5	Workshop technology	2LP11	3	1	2	6	100	40	50	20	150
6	6 Communication skills 2L12		3	1	-	4	100	40	-	-	100
	Total			6	6	30	600	-	150	-	

Semester III

a		6.1	Teaching Scheme		G 114	The	ory	Practical		Grand	
Sr. No	Course Title	Sub. code	L	Т	P	Credit (L+T+P)	$(\mathbf{I}_{+}\mathbf{T}_{+}\mathbf{P}_{+})$ Total (ESE Total		Total (and I		Grand Total
							Max	Min	Max	Min	
1	Engineering mathematics-III	3L13	3	2	-	5	100	40	-	-	100
2	Electronic measurement and instrumentation	3LP14	3	1	2	5	100	40	50	20	150
3	Management Economics	3L15	3	2	-	5	100	40	-	-	100
4	Python Programming	3LP16	3	-	2	5	100	40	50	20	150
5	Digital Logic and Circuits	3LP17	3	-	2	5	100	40	50	20	150
6	Linear Electrical Networks	3LP18	3	-	2	5	100	40	50	20	150
	Total		18	4	8	30	600	-	200	-	800

Semester IV

C		C1-		Feachi Schem	0	C 1:4	Theory		Practical		Grand
Sr. No	Course Title	Sub. code	L	Т	P	Credit (L+T+P)	Total and		Total (and I		Total
							Max	Min	Max	Min	
1	Power Electronics	4LP19	3	-	2	5	100	40	50	20	150
2	Electromagnetic and Field Theory	4L20	3	2	-	5	100	40	-	-	100
3	Microprocessor and Microcontroller	4LP21	3	-	2	5	100	40	50	20	150
4	Analog Communication	4LP22	3	-	2	5	100	40	50	20	150
5	Analog System Design	4LP23	3	-	2	5	100	40	50	20	150
6	Signals and System	4L24	3	2	-	5	100	40	-	-	100
	Total	•	18	4	8	30	600	-	200	-	800

Semester V

C		Ch		Teachi Schem	_	C 1:4	The	ory	Pract	ical	Const
Sr. No	Course Title	Sub. code	L	Т	P	Credit (L+T+P)	Total and	`	Total (and I		Grand Total
							Max	Min	Max	Min	
1	Digital Communication	5LP25	3	ı	2	5	100	40	50	20	150
2	Control System Engineering	5L26	3	2	-	5	100	40	-	-	100
3	Digital signal processing	5LP27	3	-	2	5	100	40	50	20	150
4	Embedded system and IOT	5LP24	3	ı	2	5	100	40	50	20	150
5	Printed Circuit Board	5LP29	3	1	2	6	100	40	50	20	150

	Technology-I										
6	Information Theory and coding	5L40	3	1	-	4	100	40	-	-	100
	Total		18	4	8	30	600	-	200	-	800

Semester VI

C.,		Cub		Feachi Schem	_	Credit	The	ory	Practical		Grand
Sr. No	Course Title	Sub. code	L	Т	P	(L+T+P)	Total and		Total (and I		Total
							Max	Min	Max	Min	
1	Antenna and wave Propagation	6L31	3	-	-	3	100	40	-	-	100
2	Printed Circuit Board Technology-II	6LP32	3	1	2	6	100	40	50	20	150
3	Computer Architecture and organization	6L33	3	1	-	4	100	40	1	-	100
4	Sensors & Transducers	6LP34	3	-	2	5	100	40	50	20	150
5	Software project management	6L35	3	1	-	4	100	40	-	-	100
6	Optical fiber communication	6LP36	3	-	2	5	100	40	50	20	150
7	Industrial Visit, Employability skill and Mini project lab	6P37	-	1	3	3	-	-	-	-	50
	Total		18	3	9	30	600	-	150	-	800

Semester VII

					achi	_]	Examinat	ion Schen	1e	Grand Total
Sr.		Course Title	Sub.				Credit	The	eory	Prac	ctical	
No			code	L	Т	P	(L+T+P)	To	tal	To	tal	
								Max	Min	Max	Min	
1	Digita Verilo	l system design using g	7LP38	3	-	2	5	100	40	50	20	150
2		uter network and data unication	7LP39	3	-	2	5	100	40	50	20	150
	3.1	Satellite communication	7LP40.1					100	40	50	20	150
	3.2	Mechatronics	7LP40.2									
3	3.3	Mobile and wireless communication	7LP40.3	3	-	2	5					
	3.4	Artificial intelligence and machine learning	7LP40.4									
4	Micro	wave Engineering	7L41	3	-	-	3	100	40			100
5	Projec	t Part I	7P42	1	-	6	7					100
6	6.1	Electronic product design Using EDA tools	7LP43.1	3	_	2	5	100	40	50	20	150
U	6.2	Solar installation and maintenance	7LP43.2	3	-	2	3					
			Total	16	-	14	30	500		200		

Semester VIII

G			Ck		Feachi Schem		C 1:4	The	ory	Pract	ical	Commit
Sr. No		Course Title	Sub. code	L	Т	P	Credit (L+T+P)	Total and		Total (and I		Grand Total
								Max	Min	Max	Min	
1		strial automation g PLC and SCADA	8LP44	3	1	2	5	100	40	50	20	150
2	2.1	Digital image Processing	8LP45.1	3	-	2	5	100	40	50	20	150

	2.2	Consumer Electronics	8LP45.2								
3	RAD	AR Communication	8L46	3	2	-	5	100	40		 100
4	Proje	ect	8P47	1	2	12	15				 200
		Total	•	10	4	16	30	400		100	600

4.6 Scheme of Instruction For Direct Second Year:

Every student has to register for all the subjects of a Semester as mentioned below.

Semester III

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
3B1	Power Electronics-I	3	1	2	4	100
3B2	Measurement	3	1	2	4	100
	&Instrumentation					
3B3	Computer programming	3	1	2	4	100
	C,C++					
3B4	Electronics Systems	3	1	2	4	100
	Engineering					
3B5	Engineering	3	1	0	3	75
	Mathematics-III					
3B61	General Elective-I	3	0	0	3	75
/3B62	(Commerce/Management)					
		18	5	8	22	550

Semester IV

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
4B1	Product Design	3	1	2	4	100
4B2	Power Electronics-II	3	1	2	4	100
4B3	Microprocessor	3	1	2	4	100
4B4	Integrated Circuits and Applications	3	0	2	4	100
4B5	Control System Engineering	3	1	0	3	75
4B6	Electronics Design Technology	3	1	0	3	75
		18	5	8	22	550

Semester V

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
5B1	Industrial Design of Electronic Equipment	3	1	2	4	100
5B2	Microcontroller & Peripherals	3	0	2	4	100
5B3	Digital System Design	3	0	2	4	100
5B4	Printed Circuit Board Technology-I	3	0	2	4	100
5B5	Signal and Systems	3	1	0	3	75
5B61/ 5B62	Elective-II (Obj C++ Programming / Imbedded C)	3	1	0	3	75
5B7	Industrial training/visit/internship	0	0	2	1	
		18	3	10	23	550

Semester VI

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
6B1	Transducers and sensors	3	0	2	4	100
6B2	Analog System Design	3	1	2	4	100
6B3	Printed Circuit Board	3	1	2	4	100
	Technology-II					
6B4	Industrial & Environmental	3	0	2	4	100
	instrumentation					
6B5	Software Engineering	3	0	0	3	75
6B6	Mini Project	0	0	6	3	75
		15	2	14	22	550

Semester VII

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
7B1	Digital Signal Processing	3	1	2	4	100
7B2	Embedded Systems	3	1	2	4	100
7B3	PLD and FPGA Design	3	0	2	4	100
7B4	Analog & Digital	3	1	0	3	75
	Communication					
7B51/	Elective III (Opto-	3	1	0	3	75
7B52	Electronics / Digital image					
	processing)					
7B6	Project Part I	0	0	6	3	75
		15	4	12	21	525

Semester VIII

Code	Subject	Lecture	Tutorial	Practical	Credits	Marks
8B1	VLSI System	3	1	2	4	100
8B2	System Engineering	3	1	2	4	100
8B3	Network security	3	1	2	4	100
8B41/	Elective IV (MEMS/	3	1	0	3	75
8B42	Linux OS)					
8B5	Project Part II	0	0	10	5	125

4.7 Term Course Load:

In each semester, subject load varies from 22 to 30 credits per semester. During the course period, student has to pass certain number of subjects and complete the assigned project work of 10 (ten) credits in the sixth semester satisfactorily. On valid grounds, the authority may advise a student, who is unable to complete the course requirements in the normal period, to continue for an extra term.

4.8 Assessment:

- a. A student is permitted to appear for the semester examination subject to he or she has a minimum attendance of 75% in theory and practical classes, completes all his/her sessional assignments and clears all his/her dues.
- b. Non-appearance in any examination is treated as the student having secured zero mark in that subject examination.
- c. The evaluation is based on an **average weightage system**. Every subject has credit points based on the hours of study required.

- d. Every student is assessed in a subject with equal weightage to sessional work and semester examination, thereby making the students study regularly.
- e. Every student is awarded Grade points out of maximum 10 points in each subject. (on 10 Points Scale).
- f. Based on the Grade points obtained in each subject, Semester Grade Point Average (SGPA) and then Cumulative Grade Point Average (CGPA) are computed.

Note: For computation of SGPA CGPA, refer ANNEXURE- II.

4.9 Award of Degree:

A student must complete the minimum requirement of credits in **maximum period of eight (8) years** and must obtain a **minimum CGPA of 3.3** in the course to qualify for award of Degree. The Degree is awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad.

4.10 Scholarship

The Institute encourages and provides assistance to all the students, particularly the reserved category, to apply for the Central / State Govt. scholarship for reimbursement of tuition fee and maintenance allowance as per State Govt. rules. The tuition fee is exempted for SC/ST candidates only, subject to his/her applying for the same and fulfilling the conditions.

4.11 Assistance in Placement / Pursuing Higher Studies:

The Placement Cell of the Institute offers all assistance to the students for employment / self-employment. Most of the students passing out from the Institute have good opportunities to build their career.

4.12 B.Tech Fee-Structure for 1st year admission for Academic year (2021-22)

Sr.		1st Sem. Fees &	2nd Sem. Fees (Rs.)			
No.	Particulars	Deposit (Rs.)				
1	Tuition Fee	38000	38000			
2	Caution Money Deposit *	1250	-			
	Sub Total	39250	38000			
Boy's	Hostel Accommodation	•				
3	Hostel rent per Sem. (5 months)	9100	9100			
4	Hostel Deposit*	2500	-			
	Sub Total	11600	9100			
Other	Fees					
	Particulars		Fees (Rs.)			
5	Exam Fee		100.00/- per subject/ Practical			
6	Backlog Exam Fee per subject		300.00/ per subject/practical			

^{*}Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

Important:

- i. SC/ST students are exempted from Tuition Fee (SP/TSP Scheme), only Caution Money deposit and hostel fee and deposit is to be paid.
- ii. Back log Exam Fee is applicable to all students appearing Backlog Exams.
- iii. Thereshallbeanincreaseupto10%in (Sr. No.1&3) in every academic year.

^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

4.13 B.Tech Fee-Structure for Lateral Entry admission for Academic year (2021-22)

Sr.	Particulars	3 rd Sem. Fees &	4 th Sem. Fees (Rs.)
No		Deposit (Rs.)	
1.	Tuition Fee	38000	38000
2.	Caution Money Deposit *	1250	-
	Sub Total	39250	38000
	Boy's	Hostel Accommodati	ion
3.	Hostel Fee per Sem. (5 months)	9100	9100
4.	Hostel Deposit*	2500	-
	Sub Total	11600	9100
Oth	er Fees (Additional)		
	Particulars		Fees (Rs.)
5.	Exam Fee		100.00/- per subject/ Practical
6.	Backlog Exam Fee per subject		300.00/ per subject/practical

^{*} Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

Important:

- i. SC/ST students are exempted from Tuition Fee (SP/TSP Scheme), only Caution Money deposit and hostel fee and deposit is to be paid.
- ii. Back log Exam Fee is applicable to all students appearing Back log Exams.
- iii. There shall be an increase up to 10% in (SR. No 1 & 3) in every academic year.

^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

5.0 MASTER OF TECHNOLOGY (ELECTRONICS DESIGN AND TECHNOLOGY) [M. Tech (EDT)] Full Time Course

This is four semesters (2 years) AICTE approved Postgraduate course with the Degree awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad (MS).

5.1 Eligibility/ Selection Procedure

Admission to M. Tech. degree courses will be through Centralized Counselling or M.Tech (CCMT) 2021. For details, please visit https://ccmt.nic.in/

5.2 Intake (28 Seats)

Two seats are reserved for Industry Sponsored Candidates and **three seats** are reserved for Non-Resident Indian (NRI) / Persons of Indian Origin (PIO) / Children of Indian workers in the Gulf Countries (CIWG) quota. Distribution of remaining seats is as under:

Non-Sponsored category							
Open	9						
Open- PWD	1						
EWS	2						
OBC	6						
SC	3						
ST	2						
Total	23						

Important

- a. Seats are reserved as per Govt. of India Rules, AICTE and/ or University Approval.
- b. A quota of 15 % is reserved for the SC candidates, 7.5% for ST candidates, and 27% for Other Backward Classes.
- c. Candidates selected against the quota for persons with disabilities (5%) as per PWD Act 1995 are placed in the appropriate category viz. SC/ ST/ OBC/ Open candidates depending upon the category to which they belong in the roster meant for reservation of SCs/ STs/ OBCs.

5.3 Selection Process for Admission in 1st year M. Tech (EDT) Fulltime

A) National Applicants

For Admission, please visit https://ccmt.nic.in/

Vacant seats after all rounds of CCMT 2021 will be filled in on the basis of receipt (first come first serve basis) of application form (ANNEXURE VI). However if the number of application forms exceeds the number of vacant seats, written exam will be taken to shortlist the candidates.

B) International Applicants

- i. Admission of Foreign Nationals is subject to guidelines, laid down by Government of India from time to time.
- ii. Persons of Indian Origin (PIO) is an individual with foreign citizenship, except Pakistan and Bangladesh, without "NRI" status, holding a Foreign Passport at the time of applying for admission as well as during the study period and is himself/ herself or anyone/ both of his/ her parents or anyone/ both of his/ her grandparents is/ was/ were Indian citizens.
- iii. Children of Indian workers in the Gulf Countries (CIWG) are children of an Indian who is working in Gulf Countries under relevant working visa.
- iv. Non-Resident Indian (NRI) Candidate is Child/ward of the person having 'NRI status' as defined under section 6 of the Income Tax Act.
- v. Foreign nationals may apply for admission to M. Tech (EDT) Full time course subject to fulfilling the minimum eligibility requirements through proper channel.

- vi. Their application, will however, be considered separately on receipt of application, mentioned in ANNEXURE-IV(A) on first cum first serve basis.
- vii. Foreign nationals are required to download and submit the application form for eligibility cum admission (ANNEXURE-IV(A)) and declaration & undertaking format (ANNEXURE-IV(B)) along with payment of Rs.5000/- or equivalent USD (non-refundable).

5.4 Academic Calendar – Refer ANNEXURE –I

5.5 Scheme of Instruction for First Year (2021-22): Every student has to register for all the subjects of a Semester as mentioned below.

Semester I

SI.	Course	Course Title		urs/		Total	Theory Marks		Practical	
No.	Code		wee							
			L	T	P	Credit s	ESE Marks	Internal Marks	Marks	
1.	M101	Industrial Design of	1	0	0	1	30	20	0	
		Electronic Equipment								
2.	M102	Advanced Digital System Design	3	0	0	3	70	30	0	
3.		Elective - 1	3	0	0	3	70	30	0	
4.	M103	Electromagnetic Compatibility	3	0	0	3	70	30	0	
5.	M104	Electronic Packaging	3	0	0	3	70	30	0	
6.	M105	Design for Manufacturability	3	0	0	3	70	30	0	
7.	ML101	Industrial Design of	0	0	3	3	70	30	100	
		Electronic Equipment								
		Laboratory								
8.	ML102	Advanced Digital System	0	0	2	2	40	10	50	
		Design Laboratory								
9.		Elective - 1 Lab	0	0	2	2	40	10	50	
Total			16	0	7	23	530	220	200	
Elect	ive - 1			1						
M106	6		Ma	chi	ne L	earning	<u> </u>			
M107			Networking and IOT							
Elect	ive – 1 I	_ab	•							
M106			Machine Learning Laboratory							
M107			Networking and IOT Laboratory							

Semester II

SI.	Course	Course Title	Ho	urs/		Total	Theory	Marks	Practical
No.	Code		wee	week					
			L	T	P	Credit	ESE	Internal	Marks
						s	Marks	Marks	
1	M201	Advanced Microcomputer	3	0	0	3	70	30	0
1.	141201	System Design	3	U	U	3	70	30	U
2.		Elective – 2	3	0	0	3	70	30	0
3.	M202	Mechatronics	3	0	0	3	70	30	0
1	M203	Robotics and Machine	2	0	0	3	70	30	0
7.	111203	Vision	3	U	U	3	/0	30	U
5.	M204	Embedded OS and RTOS	3	0	0	3	70	30	0
6.		Elective – 3	3	0	0	3	70	30	0

7.	ML201	Advanced Microcomputer System Design Laboratory	0	0	2	2	40	10	50				
8.	ML202	Mechatronics Laboratory	0	0	2	2	40	10	50				
9.		Elective – 2 Laboratory	0	0	2	2	40	10	50				
Total	Total			0	6	24	540	210	150				
Elect	ive – 2												
M205	M205			ASIC and SOC									
M206	M206				Mixed Signal System Design								
Elect	ive – 3												
M207	7		En	bec	lded	Applic	ations i	n Power					
			Conversion										
M208	3		Control System Design										
Elect	ive – 2 La	aboratory	I										
ML2	ML205					ASIC and SOC							
ML2	ML206				Mixed Signal System Design								

Semester III

SI.	Course	Course Title	Hours/		Total	Theory Marks		Practical	
No.	Code		wee	k				Ì	
			L	T	P	Credit	ESE	Internal	Marks
						S	Marks	Marks	
		Optical Fiber							
1.	M301	Communication	3	0	0	3	70	30	0
		System							
2.	M302	Software Engineering	3	0	0	3	70	30	0
3.	M303	Project Work and Seminar I	0	0	1 5	4	25	25	50
	MT 20	Optical Fiber							
4.	ML30	Communication	0	0	2	2	40	10	50
	1	System Laboratory							
	•	Total	6	0	17	12	205	95	100

Semester IV

SI.	Course	Course Title	Hours/		Total	Theory Marks		Practical			
No.	Code		we	week		week					
			L	T	P	Credit	ESE	Internal	Marks		
						S	Marks	Marks			
1.	M401	Project Work and Seminar II	0	0	40	20	50	50	100		
		Total	0	0	40	20	50	50	100		

5.6 Term Course Load:

- i. In each semester, subject load varies from 12 to 24 credits per semester.
- ii. On valid grounds, the authority may advise a student, who is unable to complete the course requirements in the normal period, to continue for an extra term as per M.Tech ordinances and Regulations.

5.7 Assessment:

- i. The overall performance of a student is evaluated by assigning equal weightage to all the four semesters in order to maintain the quality of education.
- ii. A student is permitted to appear for the semester examination subject to he or she has a minimum attendance of 75% in theory and practical classes, completes all his/her sessional assignments and clears all his/her dues.
- iii. Non-appearance in any examination is treated as the student having secured zero mark in that subject examination.
- iv. The evaluation is based on an average weightage system. Every subject has credit points based on the hours of study required.
- v. Every student is assessed in a subject with equal weightage to sessional work and semester examination, thereby making the students study regularly.
- vi. Every student is awarded Grade points out of maximum 10 points in each subject. (Based on 10 Points Scale).
- vii.Based on the Grade points obtained in each subject, Semester Grade Point Average (SGPA) and then Cumulative Grade Point Average (CGPA) are computed as per **ANNEXURE-II.**

5.8 Award of PG Degree:

A student must complete the minimum requirement of credits in **maximum period of four** (04) years as per M.Tech Ordinances and Regulations in order to qualify for award of Degree. The PG Degree is awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad (MS).

5.9 Scholarship

- i. Non-sponsored students, admitted to the M Tech (EDT) course, provided they have a valid GATE SCORE, are eligible for the scholarship of **Rs. 12400/-* per month**, subject to sanction and receipt of the said amount from AICTE New Delhi. Disbursement of PG-Scholarships is through direct cash transfer scheme through AICTE portal subject to his/her applying for the same and fulfilling the conditions. The award of scholarship and its continuation is subject to regular attendance, satisfactory progress, good conduct and abiding by the rules of the Institute.
- ii. Sponsored students, or students not having a valid GATE SCORE are not entitled for the said scholarship.
- iii. The tuition fee is exempted for SC/ST candidates only, subject to his/her applying for the same and fulfilling the conditions.
- iv. It is obligatory for every student, granted admission to M. Tech (EDT) and awarded scholarship, to undertake work related to teaching and research activities as assigned to him ther
- * Subject to the policies of GOI

5.10 Assistance in Placement / Pursuing Higher Studies:

The Placement Cell of the Centre offers all assistance to the students for employment / self-employment. Most of the students passing out from the Centre have good opportunities to build their career.

5.11 M.Tech. Fee-Structure, Academic year (2021-22) Admission

Sr.			Semester Fees	2nd Sem
No.	Particulars	&D	eposit(₹)	Fees (₹)
1.	Tuition Fee	460	00/-	46000/-
2.	Caution Money Deposit *	125	0	-
	Sub Total	472	50/-	46000/-
Boy'	s Hostel Accommodation	<u> </u>		
3.	Hostel Fee per Semester (5 months)		0	9100
4.	Hostel Deposit*	250	0	-
5.	Sub Total	116	600	9100
Othe	er Fees	<u> </u>		
	Particulars		Fees (₹)	
6.	Backlog Exam Fee per subject		300.00/ pe	er subject
7.	Project fee payable only in III &IV s separately	500	00	

^{*} Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

Important:

- i. SC/ST students are exempted from Tuition Fee (SCST/TSP Scheme), only Caution Money deposit and hostel fee and deposit is to be paid.
- ii. Back log Exam Fee is applicable to all students appearing Backlog Exams.
- iii. There shall be an increase up to 10% in (Sl. No. 1 & 3) in every academic year.

^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

6.0MASTER OF TECHNOLOGY (ELECTRONICS DESIGN AND TECHNOLOGY) [M. Tech (EDT)] PART TIMECOURSE

This is six semesters (3 years) AICTE approved course for working professionals with the Degree awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad (MS).

6.1 Eligibility

- i. B.E./ B.Tech Degree or equivalent in Electronics/ Electrical/ Telecommunication/ Instrumentation engineering etc. from a recognized University with at least 55% of marks.
- ii. The candidate should have been serving in Academic Institution/ Industry/ R&D organization engaged in electronic product or system development for at least two years after completion of B.E./ B. Tech degree
- iii. The candidate should be sponsored by the employer.
- iv. His/Her working place should be within 60 km distance from the institute.
- v. He should produce necessary sponsorship certificate along with application in the prescribed form given in ANNEXURE XII.

6.2 Intake: 24 Seats

6.3 Selection Process

- i. Only the Candidates meeting the eligibility criteria will be eligible for admission.
- ii. The eligible candidates have to fill the Application Form (ANNEXURE VI) and has to submit the same on **email id:** mtech-abad@nielit.gov.in
- iii. The selection for admission to M.Tech (EDT) part Time Course, will be based on **score in the written test**. List of Shortlisted Candidates will be displayed on the institute website.
- iv. Admission of the Selected Candidates will be subject to their verification of Documents and payment of applicable fees.
- v. The date and time for the waiting list counselling shall also be declared along with the list of selected candidates. All the waitlisted candidates should make themselves available at the time of the waiting list counselling, otherwise their claim shall be forfeited.
- vi. The waitlisted candidates, available at the time of counselling of the waiting list, shall be provisionally admitted as per the merit of the category-wise waiting list.
- vii. The selected merit and waiting list candidates are required to register on the day as notified along with the document and by making payment as mentioned in **Section 6.10** for admission.
- viii. The decision of Executive Director, NIELIT, Aurangabad in respect of selection and closing of admission will be final.

6.4 Admission in the event of cancellation of secured admission

If any vacancy arises due to leaving the course by a registered student after completion of admission process, the vacancy may be filled on case to case basis at the discretion of the Executive Director, by following below mentioned procedure:

- i.Preference shall be given as per the ranking in common merit list.
- ii. The Selected Students as per ranking in Merit List, who could not reach the Centre for admission on the pre-intimated day because of legal and/or genuine reason(s) and approaching/contacting the institute are first considered for filling the said vacancy.
- iii. After (i) & (ii), the candidates, who have not been offered the admission and approaching, may be considered.

6.5 Academic Calendar – Refer ANNEXURE –I

6.6 Scheme of Instruction:

Every student has to register for all the subjects of a Semester as mentioned below. **Semester I**

SI.	Course	Course Title	Но	urs/ v	veek	Total	Theory	Marks	Practical
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MP101	Electronic Packaging	3	0	0	3	70	30	0
2.	MP102	Electromagnetic	3	0	0	3	70	30	0
		Compatibility							
3.		Elective - 1	3	0	0	3	70	30	0
4.		Elective – 1 Lab	0	0	2	1	40	10	50
		Total	9	0	2	10	250	100	50
Electi	ive – 1								
MP10)3	Machine Learn	ning						
MP10)4	Networking an	d IO	T					
Electi	ive – 1 La	b							
MPL	101	Machine Learn	ning]	Labor	atory				
MPL	102	Networking an	d Io	Γ Lab	orator	y			

Semester II

SI.	Course	Course Title	Hours/ week		Total	Theory Marks		Practical	
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MP201	Advanced	3	0	0	3	70	30	0
		Microcomputer							
		System Design							
2.		Elective - 2	3	0	0	3	70	30	0
3.	MP204	Embedded OS and	3	0	0	3	70	30	0
		RTOS							
4.	MPL20	Advanced	0	0	2	1	40	10	50
	1	Microcomputer							
		System Design							
		Laboratory							
5.		Elective – 2	0	0	2	1	40	10	50
		Laboratory							
Total				0	4	11	290	110	100
Electiv	e – 2								
MP202 ASIC and SOC									
MP203 Mixed Signal System		Des	ign						
Elective – 2 Laboratory									
MPL202 ASIC and SOC									
MPL20	03	Mixed Signal System	Des	ign					

Semester III

SI.	Course	Course Title	Hours/ week		Total	Theory Marks		Practical	
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MP301	Industrial Design of	1	0	0	1	30	20	0
		Electronic							
		Equipment							
2.	MP302	Advanced Digital	3	0	0	3	70	30	0
		System Design							

3.	MP303	Design for	3	0	0	3	70	30	0
		Manufacturability							
4.	MPL30	Industrial Design of	0	0	6	3	70	30	100
	1	Electronic							
		Equipment							
		Laboratory							
5.	MPL30	Advanced Digital	0	0	2	1	40	10	50
	2	System Design							
		Laboratory							
		Total	7	0	8	11	280	120	150

Semester IV

SI.	Course	Course Title	Ho	urs/ v	veek	Total	Theory Ma	rks	Practical
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MP401	Mechatronics	3	0	0	3	70	30	0
2.	MP402	Robotics and	3	0	0	3	70	30	0
		Machine Vision							
3.		Elective - 3	3	0	0	3	70	30	0
4.	MPL40	Mechatronics	0	0	2	1	40	10	50
	1	Laboratory							
•		Total	9	0	2	10	250	100	50
Elective – 3									
		· · · · · · · · · · · · · · · · · · ·							

Elective – 3	
MP403	Embedded Applications in Power Conversion
MP404	Control System Design

Semester V

SI.	Course	Course Title	Hours/ week		veek	Total Theory Marks			Practical
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MP501	Optical Fiber	3	0	0	3	70	30	0
		Communication							
		System							
2.	MP502	Software	3	0	0	3	70	30	0
		Engineering							
3.	MP503	Project Work and	0	0	20	10	25	25	50
		Seminar I							
4.	MPL50	Optical Fiber	0	0	2	1	40	10	50
	1	Communication							
		System Laboratory							
Total				0	22	17	205	95	100

Semester VI

SI.	Course	Course Title	Hours/ week		Hours/ week		Practical		
No.	Code		L	T	P	Credits	ESE	Internal	Marks
							Marks	Marks	
1.	MPL60	Project Work and	0	0	40	20	50	50	100
	1	Seminar II							
		Total	0	0	40	20	50	50	100

Note: L: Lecture, T: Tutorial P: Practical, C: Credits

6.7 Term Course Load:

- i. In each semester, subject load varies from 10 to 20 credits per semester.
- ii. On valid grounds, the authority may advise a student, who is unable to complete the course requirements in the normal period, to continue for an extra term as per M.Tech ordinances and Regulations.

6.8 Assessment:

- i. The overall performance of a student is evaluated by assigning equal weightage to all the four semesters in order to maintain the quality of education.
- ii. A student is permitted to appear for the semester examination subject to he or she has a minimum attendance of 70% in theory and practical classes, completes all his/her sessional assignments and clears all his/her dues.
- iii. Non-appearance in any examination is treated as the student having secured zero mark in that subject examination.
- iv. The evaluation is based on an average weightage system. Every subject has credit points based on the hours of study required.
- v. Every student is assessed in a subject with equal weightage to sessional work and semester examination, thereby making the students study regularly.
- vi. Every student is awarded Grade points out of maximum 10 points in each subject. (Based on 10 Points Scale).
- vii. Based on the Grade points obtained in each subject, Semester Grade Point Average (SGPA) and then Cumulative Grade Point Average (CGPA) are computed as per ANNEXURE-II.

6.9 Award of PG Degree:

A student must complete the minimum requirement of credits in **maximum period of seven (07) years** as per M.Tech Ordinances and Regulations in order to qualify for award of Degree. The PG Degree is awarded by Dr. Babasaheb Ambedkar Marathwada University, Aurangabad (MS).

6.10 M. Tech. Fee-Structure, Academic year (2021-22) Admission

IVI. I	ech. ree-Structure, Acade	mic year (2021-22) Admis	SIOH
SR.		1 st Semester Fees &	2 nd Sem Fees (₹)
No.	Particulars	Deposit (₹)	· · · · · · · · · · · · · · · · · · ·
1.	Tuition Fee	46000/-	46000/-
2.	Caution Deposit *	1250	-
	Sub Total	47250/-	47000/-
Boy's	Hostel Accommodation		
3.	Hostel Fee per Semester	9100	9100
	(5 months)		
4.	Hostel Deposit*	2500	-
5.	Sub Total	11600	9100
Other	r Fees		
	Particulars	Fees (₹)	
7.	Backlog Exam Fee per sub	300.00/ per subject/ practical	
8.	Project fee payable only in	5000	

^{*} Caution Money Deposits are onetime payment and returnable on completion of the course subject to NIELIT rules.

^{*}Mess Service are compulsory for Hostel Students. Outside food within the premises is not permissible. Mess charges are to be paid directly to mess manager on monthly basis.

Important:

- i. SC/ST students are exempted from Tuition Fee (SP/TSP Scheme), only Caution Money deposit and hostel fee and deposit is to be paid.
- ii. Back log Exam Fee is applicable to all students appearing Backlog Exams.
- iii. There shall be an increase up to 10% in (Sl. No. 1 & 3) in every academic year.

7.0Partial List of Teaching Staff

Sr No	Name of Faculty	Designation	Educational Qualification	Brief Profile
1.	Dr. Sanjeev Kumar Gupta	Executive Director	Ph.D. (Computer Engg.), MS (Software Systems) and B.Tech (Computer Engg.)	Alumnus of BITS Pilani and NIT Kurukshetra, he is a renowned engineer, technocrat and administrator. In his professional career he is also instrumental in automation of various organizations such as Punjab State Power Corporation Limited, HSEB, CHB, ICSI, Labor Bureau. His research work is spanned across various aspects of Wireless Sensor Network. His other areas of Interest include Web Application Development, Mobile Application Development, Software Engineering, IoT, Blockchain, Big Data & Cyber Security
2.	Sh. Sasi Kumar Gera	Dean (Academics)& Scientist E	M.Tech (Manuf. Engg) and B.Tech(Mech.)	Alumnus of IIT Madras, in his professional career spanned over 24 years he is instrumental in initiating many out-of-box research works in areas of CAD/CAM, CNC Machines, Industrial Robots Machine vision, Industrial Design. He has implemented real-time robot path control by using image processing for seam-less welding applications at the University of Liverpool, England as research associate (UNDP/UNIDO fellowship). He has guided several projects at Masters level. His research interests are Industry 4.0, Autonomous Robots, CAD/CAM, Lean Manufacturing.
3.	D. Rama Rao	Scientist/Engineer-D	B.Tech (Electronics & Communications). M.Tech (Electronic Design Technology)	Overall 33 years of Experience which including 25 years of Teaching Experience to Diploma, Under Graduate, Post Graduate & Post Graduate Diploma Courses. * Subjects taught in the fields of Analog & Digital Electronics, Electronics, Measurements & Instrumentation, Service & Maintenance, Microprocessors & Microcontrollers and Linux Device Drivers. * Guided Academic Projects of the students of Diploma, Under Graduate, Post Graduate & Post Graduate Diploma Courses * Worked on Industry Sponsored & In-house R&D Projects.
4.	Sh. Lakshman	Dean (Skill Development), and Scientist D	M.Tech B.E.	In his professional career spanning over 12 years, he has executed many Government Projects of IT Mission (Kerala), Ministry of Social Justices, and ISEA project etc. His areas of areas of interest are Thermal Image Processing, Blockchain, Cyber Security, Mobile Application Development and Software Engineering. He is also working as a Placement Officer and Nodal Officer of Model Career Centre.
5.	Sh. Y. A. Khan	Sr. Principal Programmer	M.C.A.	Experienced Software Professional. Developed the projects for Office

Sr No	Name of Faculty	Designation	Educational Qualification	Brief Profile	
				Automation. Well versed with Database techniques and Software Engineering Practices.	
6.	Sh. D.S. Raje	Scientist C	B.E.(Electronics)	He has over 27 years of experience as Electronics Engineer and excels in the field of Test and Measurement.	
7.	Sh. Saurabh Kesari	Scientist C	B.Tech (Electronics and Tele- Communication Engineering)	More than 6 years of industrial experience in Embedded and IOT Hardware design and development	
8.	Sh. Saurabh Bansod	Scientist B	M.Tech(Electronics & Instrumentation) B.E.(Electronics)	Alumnus of N.I.T. Rourkela, In the span of 18 months he has done tremendous work in the area of Industrial Automation. His area of interest includes data acquisition using NI DAQ cards.	
9.	Sh. Prashant Pal	Scientist B	M.Tech, B.Tech	With expertise in Electronics System design, he has experience of teaching advanced microcontroller and microprocessor. He has sound knowledge of Deep learning and Machine learning. He is also doing projects on Artificial Intelligence, Visual Information and Embedded Systems from IIT Kharagpur.	
10.	Sh. Yogesh	Scientist 'B'	B.Tech (CSE)	A young scientist who possesses expertise in the area of Internet of Things, Scripting languages like Python. His other areas of interest are Cyber Security, Web Application Development.	
11.	Sh. Ashwini Vishwakarma	Scientist 'B'	B.E. (Electronics and Communication Engineering)	A young scientist who possesses expertise in the area of Internet of Things, Scripting languages like Python. More than 2 years of teaching experience.	
12.	Sh. Shashank Kumar Singh	Scientist 'B'	B.Tech. (Electronics and Communication Engineering)	A young scientist who possesses expertise in the area of VLSI. More than 1 years of teaching experience.	
13.	Sh. B. B. Sorte	Sr. Tech. Officer	DME, (DCS&M)	More than 20 Years' experience as Trainer / faculty of CAD/CAM/CAE including 08 Years of experience as Faculty for Mechanical Design and Developments and Workshop Technology. He is looking after Design & Development of Electro-Mechanical products under Academic activities of DEPM & B.Tech & M.Tech courses	
14.	Sh. M. S. Kshirsagar Sh. Milind Garud	Sr. Tech. Officer Sr. Tech. Officer	Diploma (Ind. Electronics) Diploma (Ind. Electronics)	He is highly motivated and experienced faculty who specializes in Electronics. About 29 Years' experience in Power Electronics and conducting of lab/practical's. He is also looking after the examination related activities and academic for about 15 years. Also working as NSS Officer for past 4	
16.	Sh. Kishor Chaudhari	Sr. Tech. Officer	BCA, CCNA, CCNP	Years. Specialization in VPN technologies, Routing & Switching, VOIP, Switched Network Design. Area of Interest is MPLS, SNMP,	

Sr	Name of	Designation	Educational	Brief Profile		
No	Faculty		Qualification			
				Network security, IPS, IDS, and Data Center.		
17.	Sh. Th. Sunil	Principal Technical	BE(ECE)	He is interested learning new trends in		
	Kumar Singh	Officer		Technologies in his area. He has more than 20		
				years of undergraduate teaching		
				microprocessor and Microcontrollers.		
18.	Sh.	Senior Technical	B.Tech (Electronics	With expertise in Electronics System design,		
	Suryacharan	Assistant	and communication.)	he has experience of teaching various subjects		
				of electronics. He has also worked as program		
				analyst in cognizant for 2 years on ETL		
				testing, SQL, Informatics and MSTR. His		
				area of interest includes Microelectronics, AI		
				and data acquisition using NI DAQ cards.		
19.	Sh. Pawan	Senior Technical	B.Tech (Electronics	Expertise in VLSI design (Ngspice, VHDL,		
	Kumar Patel	Assistant	and communication.)	Verilog, System Verilog, Blue spec),		
				Scripting languages like Python. More than 1		
				years of teaching experience.		

8.0 Placement Assistance and Support: Students of the Centre are trained to become R&D engineers. In Course curriculum there is emphasize on Innovation, Design and Development of Electronic Product. The Centre has also signed MoU with Chamber of Marathwada Industries and Agriculture (CMIA) to platform to Startup Aspirants students. In association with Directorate of Employment, Ministry of Labour & Employment (MoLE), a Model Career Centre is also functioning to provide a variety of employment related services. Apart from this an independent Placement Cell is providing Placement support and assistance to all the students. Almost all the students of the Institute gets career opportunities of their choice.

1. MoU with CMIA



CMIA is a group organization representing around 650 small scale / medium scale / large scale industries including the Multinational Companies (MNC's) of the Maharashtra. An MoU was signed with CMIA in November, 2017 for referral of Students Projects which have potential of developing into scalable business models and also adoption of their business startup ideas. The support for internship and employment to our students in member companies of CMIA was another goal of the MoU.

2. Model Career Centre





In association with Directorate of Employment, Ministry of Labour and Employment (MoLE), NIELIT is providing a variety of employment related services to students of the region. The students of the institute are by default members of National Career Services (NCS) of Government of India. The Model career Centre apart from organizing multiple Job Fairs every year is also conducting counseling sessions to improve Soft Skills and presentation skills of the students. Leading Experts and Industrialists are

invited for the counseling sessions to share their views.

3. Industrial Tie-up

Multiple visits of the students are arranged in leading Industries of the region so that they can get well versed with current Industrial trends. The students also get a chance to take up real Industrial issues as their project work. The bright students are also provided with mentoring support for establishment of their own start-up by Industrialists.



4. Some of Companies who have come from Campus Placement



































9.0 Some of the Alumni of the Centre

NIELIT Aurangabad believes in developing and maintaining a strong alumni association for its growth and progress

1. Dr. Suresh D. Shirbahadurkar



Professor Zeal College of Engineering, Narhe, Pune

"Progress Seminars Conducted by NIELIT Aurangabad research centre and attended by fellow researches, M.Tech Students & eminent guides provided me a forum to present and discuss my research. All the IEEE publications were available for reference. The state of art lab facilities were available for simulation & experimentation."

2. Dr. Radhakrishna Naik



Vice Principal G S Mandals Maharashtra Institute of Technology Aurangabad

"The industrial Design & Product Design subjects helped me to compliment my class room learning with in-depth project work. Guest lectures arranged at NIELIT exposed us to latest trends in industry & real life problems. Industrial visits helped us to understand & relate our subject to industrial environment"

3. Dr Varsha Ratnaparkhe



Assistant Professor & Dean (Quality Assurance), Department of Electronics & Telecommunication Engineering, Government College of Engineering, Aurangabad "Skills that I acquired and honed while in NIELIT Aurangabad, are benefiting me continuously in my professional career. NIELIT has helped me shape my character and strengthened attitude required to deliver strong results in academia."

4. Mr. Sumit Wankhad



VLSI Engineer, Cerium Systems, Bangalore

"I found, NIELIT Aurangabad atmosphere conducive for learning. NIELIT Aurangabad helped in building strong fundamentals with deeper understanding in Electronics Product Design. A number of facilities including labs were accessible to students. Faculty were readily available to solve any study related difficulties and staffs were very kind in resolving any related issues."

5. Dr. Alka Mahajan



Director Nirma University, Indore

"NIELIT Aurangabad taught me to think critically and confidently in experimental and theoretical situations. I developed professionally and made a wealth of friends and resources".

6. Mr. Jaykumar H Prabhakar



Vice President (Global lead incident management) at Accenture, Thane. Also a Member of ISKCON working with NGO for Swachh Bharat

"What makes this course unique are the subjects in product design and PCB design which helped me understand the whole process of product development Making of the product was a very creative experience with starting from design, to manufacturing of PCB in the PCB Lab & then making the enclosure in the workshop, not to forget the innumerable sketches we made of the various versions & forms of the product."

7. Arvind B Nyayadhish



Director Enman Automation Pvt.Ltd, Aurangabad

"To shine in today's competitive world it is very essential to have the nurturing that helps you go the extra mile. NIELIT Aurangabad equipped me for the world outside with the best skill set. Those amazing years gave me much more than bookish knowledge; I met probably the best people in my life and some inspiring personalities Proud to be an alumnus of NIELIT Aurangabad."

8. Mr. Mahendra Padalkar



Principal Technical Architect (Cloud)at Tech Mahindra Ltd, Pune "In NIELIT Aurangabad, I acquired and honed not only technical skills but also management and people skills that are assisting me immensely in my career. I'm thankful to NIELIT Aurangabad for providing such a strong foundation towards my career."

9. Mr. Pradeep Kizhiseeri



Senior Consultant Presently into Hatstand, Singapore

"NIELIT Aurangabad is where the students are molded to Perfect Industry Professionals & Entrepreneurs. The reputation and brand equity associated with the institute makes one feel proud. Thanks to college management and faculty for engineering my career in right direction."

10. Mr. Sandeep K Patni



Co-Founder and VP of Systems and Engineering at CumuLogic Inc, New Jersey, USA

"NIELIT Aurangabad taught me that education can be the most challenging, extremely rewarding, exciting, and fun. I learned that passion for learning really is the driver of finding new knowledge, and that passion is honestly contagious."

11. Mr. Rupesh Kollale



President & Director Endress+Hauser Infor Serve (India) Pvt. Ltd. Aurangabad

"NIELIT (CEDTI), provides the perfect platform for students to excel 'Beyond the theory' to work and experiment with latest technological things, this is a world class environment right here in Aurangabad where there is freedom to hone your practical skills which are very important along with the theory. We had very supportive and passionate teachers who made us what we are today. I am immensely thankful to NIELIT for shaping my life."

13. Mr. Hrushikesh Gangur



Sr. Solutions Architect, Amazon Web Services, San Francisco, California

"It is close to 25 years, and I still have memories of those golden days that made me a complete man. The education, labs and end-to-end understanding of product lifecycle learnt for CEDTI (now known as NIELIT) still help me in day-to-day work and life. I am blessed that I had my education done from this institute. I wish other engineering colleges have a same bar raising faculties, facilities, and methodology as NIELIT has to build quality engineers for India."

10.0 Refund of fees in the event of cancellation of admission:

- 1. If a candidate after accepting the offer wishes to withdraw from the admission process, Deposited fee will be refunded after deducting Rs.1500/- towards application processing fee. Provided the withdrawal is made on or before 1st October 2021. Candidate must send an email to depm-abad@nielit.gov.in / btech-abad@nielit.gov.in with subject Refund, for claiming refunds towards withdrawal from course giving Application Number, Name, etc. Refund of fees for M.Tech (First Semester) will be in accordance to CCMT-2021. For more details see M.Tech Ordinances and Regulations, B.Tech Ordinances and Regulations and DEPM Ordinances and Regulations
- 2. Seat booking fee includes tuition fee and hostel fee.
- **3.** In case of any discrepancy, the decision of Executive Director, NIELIT, Aurangabad in respect of refund of fees in the event of cancellation of admission will be final

ANNEXURE I

Tentative Academic Calendar for M.Tech (EDT), B.Tech (ESE) and DEPM Programs Academic Year 2021-2022 (Semester I)

Sr. No.	Semester-I					
1	Start of Online application	14 th August 2021				
2	Last date of Online application	10 th Sept. 2021				
3	Instruction Begins	1st Oct. 2021				
4	Class Test-1	15 th Nov 2021*				
5	Class Test-2	15 th Dec 2021*				
6	Instruction Ends	31st Dec 2021*				
7	Semester (Practical) Examination	1 st Jan 2022*				
8	Semester (Theory) Examination	10 th Jan 2022*				
9	Project Assessment	10 th Jan 2022*				
	Project Feasibility Seminar					
10	Semester Break (DEPM and B.Tech)	20th Jan 2022 to 31st Jan 2022*				
11	Declaration of Results	31st Jan 2022*				

^{*} Tentative Dates.

<u>ANNEXURE – II</u>

Assessment Computation of SGPA & CGPA

- 1. **Semester Grade Point Average (SGPA)** is the weighted average of Grade Points obtained by a student in a semester. Details are given in M.Tech, B.Tech and Diploma Ordinances and Regulations
- 2. **The Cumulative Grade Point Average (CGPA)** is used to describe the overall performance of a student in a Post Graduate/ Graduate/ diploma programme. Details are given in M.Tech, B.Tech and Diploma Ordinances and Regulations.

Note: The Semester and Cumulative GPA are rounded off to the second place of decimal

ANNEXURE III

	NIELIT	Aurangabad	l, Maharashtr	a (India)					
			ation form						
				ar) of 3 Year's and Maintenance	e)				
DEPM (Diploma in Electronics Production and Maintenance)									
To, The Dean Acaden Aurangabad, Dr. BAM Univers Aurangabad, 4310			Passport Size Recent Photogra Attested (Size 4.5x5.5 cm)	ph					
Sir/Madam, I have passed XII stand Board with Physics, Chen hereby applying for Direct (DEPM) Course during the selection test for the said co	nistry, Math t admission e Academic	s OR ITI (Eleto 3 rd Semeste year 2020-202	ectrical / Electronical / Electronic	ronics) from recog Electronics Product you to kindly allov	gnized Institute. I am tion and Maintenance w me to appear in the				
Name of Candidate:									
Mother's Name									
Father's Name:									
Date of Birth:									
Category [General/SC/ST PWD(General)/PWD(OE									
		National Inst	itute of Electro	nics and Informati	on Technology				
Name of the Institute/Ben	eficiary	(NIELIT)							
Name of the Bank		State Bank of India							
Branch		Samarth Nagar Aurangabad Maharashtra							
Saving Bank Account Nu	mber	32078399585							
IFSC/RTGS NO		SBIN 0007919							
Mode of Electronic Trans	fer	NEFT, SBICollect, Website: www.onlinesbi.com							
Application Fee		The application fee is Rs.500/ However, the candidates belonging to SC/ST/PWD are exempted from application fees.							
Address for Correspond	ence:								
		Pin:							
E-mail ID:		Landline No.	:	Mobile No.:					
Total % marks in ITI or			-		1				
ITI Year	% Marks	1	12 th standa	rds subject	% Marks				
1 st Year			Physics						
2 nd Year			Chemistry						
			Maths						
A C 1			Vocational						
Average of above two years			Average of subjects	any above three					

Candidate Signature with date

Important Instructions

- 1. Form should be signed by the student.
- 2. Incomplete form will not be accepted.
- 3. Mail scanned copy of filled form & fee receipt to depm-abad@nielit.gov.in
- 4. Please attach the scan copy of fee deposit counter along with application form

ANNEXURE- IV(A)

Application Form for Eligibility cum Admission to DIPLOMA / B.Tech/M.Tech Full Time for Foreign Nationals

To,

The Dean Academics, NIELIT Centre Aurangabad, University Campus, Aurangabad 4310004 (MS) India

Telephone: 91(0240) 2982021,2982022, 2982050(Fax)

Website: www.nielit.gov.in/aurangabad

Important Instructions

- 1. Form should be signed by the student.
- 2. Incomplete form will not be accepted.
- 3. No refund of Application form Fees.
- 4. Mail scanned copy of filled form& fee receipt to respective E-mail: depmabad@nielit.gov.in, btech-abad@nielit.gov.in, mtech-abad@nielit.gov.in

Sir/Madam,

I hereby apply for grant of eligibility and admission as an International Student to Diploma in Electronics Production and Maintenance (DEPM) /B.Tech (EDT) / M.Tech course during the Academic year and request you to kindly grant me a certificate of eligibility and admission to the said course in NIELIT Centre, Aurangabad, Maharashtra (India). I submit my particular asunder:

CANDIDATE'S DETAILS

Passport Size Recent
PhotographAttested
(Size:4.5x5.5cm)

Last Name: First Name:	Middle Name:	Mother Name:	Date of Birth:	DD/MM/	YYYY	Nationality

ADDRESS FOR CORRESPONDENCE											
						Pi	in:				
E-mail ID: Tel No. (with ISD/STD)											

	ACADEMIC QUALIFICATIONS (in ascending order)									
Sr.	Examination	Name of	Name of	Year of	% Marks	Class /				
No.	Passed	School / College	Examining body	Passing	obtained	Division				
		_	(Board / University)							

QUALIFYING EXAMINATION DETAILS							
10 th Std. Ma	rks / Grade (Fo	GATE or Equivalent Score Details (if applicable) (For M.Tech (EDT) / Ph.D)					
Subject	Science	Year	Discipline	Percentile			
Marks / Grade Obtained							
Maximum Marks							

	WORKING EXPERIENCE
Name of Industry / Institution	
Type of Work / Experience	
Experience in years	

Passed X std. or higher level Examination with English as one of the passing subjects

Name and address of the School / College / Institution last attended

Details for online fee payment for DIPLOMA/ B.Tech/ M.Tech Full Time for Foreign Nationals Students are as given below.								
Bank Account No 20060526862								
Account Type	Current a/c							
Account Name	National Institute of Electronics and Information Technology (NIELIT), Aurangabad							
Bank Name& Address	Bank of Maharashtra, Dr. B.A.M. University branch Aurangabad (MS)							
IFSC Code	MAHB0000152							
Mode of Electronic Transfer	NEFT, RTGS							

	Check List (Please attach Attested photocopies of all the Certificates for Sr. No. 2 to 6 below)											
01.	Two Passport Size Photograph pasted & attested YES NO											
02	Date of Birth proof, copy attached (X Mark-sheet / Certificate) YES NO											
03	Caste (OBC/SC/ST) Certificate, copy attach YES NO											
04	04 Disability Certificate for PWD, copy attached YES NO											
05	12 th /Graduation Passing Certificate, copy attached YES NO											
06												
07	Qualifying Degree Certificate, copy attached	YES	NO									
08	GATE Score Card, copy attached (M.Tech Full Time)	YES	NO									
09	9 Sponsorship letter Original / Experience letter attached YES NO											
10	Payment receipt in the form of RTGS/NEFT Enclosed YES NO											
	Note: The application form is liable to be rejected if found incomplete or if the necessary & appropriate documents											

& Payment are not enclosed along with.

CANDIDATE SIGNATURE:

EOD	OFFICE	TICT	ONIT	T 7

Registration No			Application Form No			
					i I	ı

Checked By:

Academic Section I/C M.Tech Coordinator Dean Academics B.Tech Coordinator Diploma Coordinator

Date: DD /MM /YYYY

ANNEXURE-IV (B)

(To be typed on Rs.100/- Stamp Paper) Declaration and Undertaking

- 1. I hereby declare that I have carefully read this application form for eligibility and admission and have noted the instructions / requirements thereby.
- 2. I have also carefully noted the rules of eligibility & conduct and discipline, laid down by the NIELIT Centre, Aurangabad and I agree to abide by them.
- 3. I understand and declare that I shall be responsible for any discrepancies, error, wrong or incorrect information, supplied by me in this application form and for cancellation of admission thereby or otherwise found ineligible.
- 4. I undertake to furnish the necessary certificate(s)/ document(s)/ paper(s) in original along with a true copy of each of them as and when asked for, failing which I understand that my eligibility and admission stands automatically cancelled and that the NIELIT Centre, Aurangabad is not responsible for the same.

I hereby de	clare th	iat th	ie infor	matic	n fur	nished t	y n	ne in	this	form is	true	and	correct	to the	bes	st of
my knowle	edge. I	am	liable	to b	e disc	_l ualified	l if	the	com	petent	autho	rity	notices	that	Ił	ave
furnished as	ny false	e info	ormatio	n.												

Date: Place:

	Yours Faithfully,
(Name & Signature of	f Foreign National)

ANNEXURE-IV (C)

(To be typed on Rs.100/- Stamp Paper) Declaration and Undertaking

- 1. I hereby declare that I have carefully read this application form for eligibility and admission and have noted the instructions / requirements thereby.
- 2. I have also carefully noted the rules of eligibility & conduct and discipline, laid down by the NIELIT Centre, Aurangabad and I agree to abide by them.
- 3. I understand and declare that I shall be responsible for any discrepancies, error, wrong or incorrect information, supplied by me in this application form and for cancellation of admission thereby or otherwise found ineligible.
- 4. I undertake to furnish the necessary certificate(s) / document(s) / paper(s) in original along with a true copy of each of them as and when asked for, failing which I understand that my eligibility and admission stands automatically cancelled and that the. NIELIT Centre, Aurangabad is not responsible for the same.

I hereby declare that the information furnished by me in this form is true and correct to the best of my knowledge. I am liable to be disqualified if the competent authority notices that I have furnished any false information.

furnished any false information.	
	Yours Faithfully
	(Name & Signature of Candidate)
	(Name & Signature of Guardian/Parent)
Date:	

Place:

ANNEXURE V

NIELIT Aurangabad, Maharashtra (India)							
Application form							
Lateral Entry Admission (Direct 2 nd Year) of 4 Year's							
B.TECH (Electronics System Engineering)							
Го,							
The Dean Academics, NIELIT Aurangabad, Dr. BAM University Campus, Aurangabad, 4310004 (MS)	,	Passport Size Recent Photograph Attested (Size: 4.5x5.5 cm)					
Sir/Madam, Ihavepassed3yeardiplomacourseinElectronics&alliedstreamswithminimum45%marks (40 percent for SC/ST candidates) approved by AICTE. I hereby register for admission to 3rd Semester B.Tech (Electronics System Engineering) Course through Lateral Entry during the Academic year 2021-22 and request you to kindly grant me admission to the said course at NIELIT Aurangabad. I submit my particular as under:							
Name of Candidate:							
Mother's Name							
Father's Name:							
Date of Birth:							
Category [General/SC/ST/OBC /PWD(General)/PWD(OBC)]							
Name of the Institute/Beneficiary	National Institute of Electronics and Information Technology						
Name of the Bank	State Ban	ık of India					
Branch	Samarth 1	Nagar Auranga	abad Maharashti	ra			
Saving Bank Account Number	32078399	9585					
IFSC/RTGS NO	SBIN 000	07919					
Application Fee	The application fee is Rs.500/ However, the candidates belonging to SC/ST/PWD are exempted from application fees.						
Mode of Electronic Transfer NEFT, SBICollect, Website: www.onlinesbi.com							
Address for Correspondence:	, , , ,						
radicis for correspondence.							
	Pin:		•				
	Landline		Mobile No	.:			
Total % marks in Diploma Course in Engineering and Technology							
Branch/Discipline		1st Year %	2 nd Year %	3 rd Year %	Avg. %		

Candidate Signature with date

Important Instructions

- 1. Form should be signed by the student.
- 2. Incomplete form will not be accepted.
- 3. Mail scanned copy of filled form &fee receipt to https://doi.org/10.1007/journal.org/
- 4. Please attach the scan copy of fee deposit counter foil along with application form.

ANNEXURE VI

NIELIT A	ırangahad	, Maharashtra	(India)		
NIELITA			(IIIuia)		
Application form 2 year/ 3 Year's M.Tech (Electronics Design Technology) Full time/ Part Time Course Admission					
То,					
The Dean Academics, NIELI' Aurangabad, Dr.BAM University Campus, Aurangabad, 4310004(MS)		Passport Size Recent Photograph Attested (Size: 4.5x5.5 cm)			
Sir/Madam,			1		
I have passed B.E./B.Tech Degramstrumentation engineering etc. from the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology) Proportion of the marks (50 percent for SC/ST cand (Electronics Design Technology)	rom a reco lidates). I a	gnized Universum hereby app	sity with a minimum lying for the admission	of 55 percent on to M. Tech	
Name of Candidate:					
Mother's Name					
Father's Name:					
Date of Birth:					
Category [General/SC/ST/OBC /PWD(General)/PWD(OBC)]					
Sponsorship by Academic Institute/Industry					
Working Experience					
Approximate Distance of Working place from the Institute (Kms)					
Name of the Institute/Beneficiary	National Ir (NIELIT)	stitute of Elect	ronics and Information	Technology	
Name of the Bank	State Bank	of India			
Branch	Samarth N	agar Aurangab	ad Maharashtra		
Saving Bank Account Number	320783995	85			
IFSC/RTGS NO	SBIN 0007	919			
Mode of Electronic Transfer	NEFT, SB	Collect, Webs	ite: www.onlinesbi.com	n	
Application Fee			Rs.500/ However, to are exempted from ap		
Address for Correspondence:					
	Pin:				
E-mail ID:	Landline N	lo.:	Mobile No.:		

Total % marks in B.Tech/B.E Degree in Electronics Engineering or allied streams					
Stream/Discipline	1st Year %	2nd Year %	3rd Year %	4th Year %	Avg. %

Tick Appropriate cell based on category and hostel accommodation						
Amount to be paid on counseling for admission (1st Semester M.Tech Fee & Deposits)						
Category Institute Fee Institute Hostel fee (in case hostel required)						
All other than SC/ST	Rs: 47,250/-	Rs: 11600/-				
SC/ST	Rs: 1250/-	Rs:11600/-				

Following documents with one self-attested copy of each document to be handed over to NIELIT Aurangabad academic section at the time of admission depending upon the category to which the candidate belongs.

Documents (Original with Self attested copy)	Certificate No. & Date of Issue	Yes/No	Checked (By Office)
Two Passport Size Photograph (attested)			
Date of Birth proof (X Mark-sheet / Certificate)			
All Mark Lists of the Qualifying Examination			
Degree Certificate of the Qualifying Examination.			
Conduct Certificate from the College, where the student has last studied			
Transfer Certificate from the college last studied.			
Migration Certificate (In case students are from other university)			
Physical Fitness Certificate (as per given format)			
Non creamy layer OBC certificate valid up to 31st March 2022, as per given format (OBC candidate only)			
SC/ST Certificate as per given format (SC/ST candidate only)			
Physical With Disability Certificate as per given format (PWD candidate only)			
Sponsorship Certificate and Experience Certificate (Sponsored Candidates Only)			

I hereby declare that the information furnished by me in this form is true and correct to the best of my knowledge. I am liable to be disqualified if the competent authority notices that I have furnished any false information. I am ready to remit Rs....../- to bank as per the details given above today itself to secure the admission.

Candidate Signature with date

Important Instructions

- 1. Form should be signed by the student.
- 2. Incomplete form will not be accepted.
- 3. Mail scanned copy of filled form &fee receipt to mtech-abad@nielit.gov.in
- 4. Please attach the scan copy of fee deposit counter foil along with application form

ANNEXURE VII Prescribed Performa for SC/ST Certificate

	fumari* son/daughter of
of village/town/* in D	
	which is recognized as a Scheduled Castes [SC]*
/ Scheduled Tribes [ST]* under:	
The Constitution (Scheduled Castes) Or	·
The Constitution (Scheduled Tribes) Or	der, 1950
The Constitution (Scheduled Castes) Un	nion Territories Order, 1951
The Constitution (Scheduled Tribes) Un	nion Territories Order, 1951
the Bombay Reorganization Act, 1960 & Himachal Pradesh Act 1970, the North-Scheduled Castes and Scheduled Tribes O The Constitution (Jammu & Kashmir) (Andaman and Nicobar Islands) Schedule Castes and Scheduled Tribes Order (Am Nagar Haveli) Scheduled Castes Order, Scheduled Tribes Order 1962**. The Constitution (Scheduled Constitution (Goa, Daman & Diu) Scheduled Constitution (Goa, Daman & Diu) Scheduled Tribes Order, 1970**. The Constitution (ST) Orders (ST) Orders (Second Amendment) Act, 1 Ordinance, 1996. The Scheduled Caste an The Constitution (Scheduled Caste) Orders (Second Caste) Orders (Scheduled Caste)	Scheduled Castes Order, 1956. The Constitution d Tribes Order, 1959 as amended by the Scheduled endment Act), 1976. The Constitution (Dadra and 1962. The Constitution (Dadra and Nagar Haveli) onstitution (Pondicherry) Scheduled Castes Order, Tribes) (Uttar Pradesh) Order, 1967**. The uled Castes Order, 1968**. The Constitution (Goa, 1968**. The Constitution (Nagaland) Scheduled likkim) Scheduled Castes Order, 1978**. [%] ribes Order, 1978**. The Constitution (Jammu & The Constitution (SC) Orders (Amendment) Act, Amendment) Ordinance, 1991**. The Constitution (991**. The Constitution (ST) orders (Amendment) act, 2002. The Constitution Orders (Amendment) Act, 2002. The Constitution Orders (Amendment) Act, 2002. The Constitution
migrated from one State/Union Territor This certificate is issued on the basis certificate issued to Shri/Shrima Father/Mother of Shri/Srimati/Kumari* of village/town* in the District/Division the Caste/Tribe* which is recognized a State/Union Territory* issued by the da 3. Shri/Shrimati/Kumari* and/or* village/town* of	s of the Scheduled Castes / Scheduled Tribes hti * a* of the State/Union Territory*, who belong to his a Scheduled Caste* / Scheduled Tribe* in the hted. % his/her* family ordinarily reside(s) in the
of.	District/Division* of the State/Union Territory
of	
Place	Signature
Date	Designation
(with seal of office)	Designation
* Please delete the words which are not	annlicahla
** Please quote specific presidential ord	

⁵¹

% please delete the paragraph which is not applicable.

^ List of authorities empowered to issue Schedule Caste / Schedule Tribe Certificates:

- 1) District Magistrate / Additional District Magistrate / Collector / Deputy Commissioner / Additional Deputy Commissioner / Deputy Collector / 1st Class Stipendiary Magistrate / Sub-Divisional Magistrate / Extra-Assistant Commissioner / Taluka Magistrate / Executive Magistrate.
- 2) Chief Presidency Magistrate / Additional Chief Presidency Magistrate / Presidency Magistrate.
- 3) Revenue Officers not below the rank of Tehsildar.
- 4) Sub-Divisional Officers of the area where the candidate and/or his family normally resides.

NOTES:

1) The term ordinarily reside(s) used here will have the same meaning as in Section 20 of the Representation of the People Act, 1950.

ANNEXURE VIII OBC Caste Certificate Format

[This certificate MUST have been issued on or after 1st April 2021]

This is to certify that Shri/Smt./Kum. _____Son/Daughter of Shri/Smt. _____ of Village/Town District/Division in the State/UT belongs to the Community which is recognized as a backward class under:

- (i) Resolution No. 12011/68/93-BCC(C), dated 10/09/93 published in the Gazette of India Extraordinary Part I Section I No. 186, dated 13/09/93.
- (ii) Resolution No. 12011/9/94-BCC, dated 19/10/94 published in the Gazette of India Extraordinary Part I Section I No. 163, dated 20/10/94.
- (iii) Resolution No. 12011/7/95-BCC, dated 24/05/95 published in the Gazette of India Extraordinary Part I Section I No. 88, dated 25/05/95.
- (iv) Resolution No. 12011/96/94-BCC, dated 9/03/96.
- (v) Resolution No. 12011/44/96-BCC, dated 6/12/96 published in the Gazette of India Extraordinary Part I Section I No. 210, dated 11/12/96.
- (vi) Resolution No. 12011/13/97-BCC, dated 03/12/97.
- (vii) Resolution No. 12011/99/94-BCC, dated 11/12/97.
- (viii) Resolution No. 12011/68/98-BCC, dated 27/10/99.
- (ix) Resolution No. 12011/88/98-BCC, dated 6/12/99 published in the Gazette of India Extraordinary Part I Section I No. 270, dated 06/12/99.
- (x) Resolution No. 12011/36/99-BCC, dated 04/04/2000 published in the Gazette of India Extraordinary Part I Section I No. 71, dated 04/04/2000.
- (xi) Resolution No. 12011/44/99-BCC, dated 21/09/2000 published in the Gazette of India Extraordinary Part I Section I No. 210, dated 21/09/2000.
- (xii) Resolution No. 12016/9/2000-BCC, dated 06/09/2001.
- (xiii) Resolution No. 12011/1/2001-BCC, dated 19/06/2003.
- (xiv) Resolution No. 12011/4/2002-BCC, dated 13/01/2004.
- (xv) Resolution No. 12011/9/2004-BCC, dated 16/01/2006 published in the Gazette of India Extraordinary Part I Section I No. 210, dated 16/01/2006.
- (xvi) Resolution No. 12015/2/2007-BCC, dated 18/08/2010.
- (xvii) Resolution No. 12015/2/2007-BCC, dated 11/10/2010.
- (xviii) Resolution No. 12015/13/2010-BC-II, dated 08/12/2011.
- (xix) Resolution No. 12015/05/2011-BC-II, dated 17/02/2014.
- (xx) Resolution No. 12011/6/2014-BC-II, dated 07/12/2016.
- $(xxi)\ Resolution\ No.\ 12011/13/2016\text{-BC-II},\ dated\ 22/12/2016$
- (xxii) Resolution No. 20012/1/2017-BC-II, dated 19/01/2017
- (xxiii) Resolution No. 12011/7/2017-BC-II, dated 31/07/2017

Shri/Smt./Kum.		and/or	his	family	ordinarily	reside(s)	in
the							
District/Division of _			State/	UT. This is	s also to certify	y that he/she	does
not belong to the pe	ersons/sections	(Creamy Lay	v er) mer	ntioned in C	Column 3 of th	ne Schedule t	o the
Government of India	, Department of	Personnel &	Training	g O.M. No.	36 012/22/93	-Estt.(SCT),	dated
08/09/93 which is	modified vide	OM No. 360	033/3/20	04 Estt.(R	es.), dated 09	0/03/2004, fu	ırther
modified vide OM N	To. 36033/3/2004	4-Estt. (Res)	dated 14	1/10/2008,	again further n	nodified vide	OM
No. 36036/2/2013-Es	tt (Res) dated 30	0/05/2014.					

Place Signature Date Designation

(with seal of office)

NOTE:

- (a) The term 'Ordinarily' used here will have the same meaning as in Section 20 of the Representation of the People Act, 1950.
- (b) ^The authorities competent to issue Caste Certificates are indicated below:

- (i) District Magistrate / Additional Magistrate / Collector / Deputy Commissioner / Additional Deputy Commissioner / Deputy Collector / First Class Stipendiary Magistrate/ Sub-Divisional magistrate / Taluka Magistrate / Executive Magistrate / Extra Assistant Commissioner (not below the rank of 1st Class Stipendiary Magistrate).
- (ii) Chief Presidency Magistrate / Additional Chief Presidency Magistrate / Presidency Magistrate.
- (iii) Revenue Officer not below the rank of Tehsildar.
- (iv) Sub-Divisional Officer of the area where the candidate and / or his family resides

ANNEXURE IX Physical Disability Certificate (format)

Certificate No.	Photograph Of
This is to contifue that I have a various d	the
This is to certify that I have examined Mr./MsSon/Daughter/Wife of MrAge Genderon	Candidate Showing the Physical
 i. He/ She is suffering fromwhich comes unde Blindness /Low vision/Speech & Hearing impairment/Orthopedic disabilities. Dyslexia, Dyscalculla, Dysgraphica, Spastic. ii. The percentage of disability is%. iii. The disability is permanent in nature. 	
iv. This condition is progressive/non-progressive/likely to improve/not Reassessmentofthiscaseisnotrecommended/isrecommendedafteraperiodofyearsmonths.	
v. The candidate is capable of carrying out all activities related to theory an applicable to DEPM/B.Tech/ M.Tech course of NIELIT Aurangabad concession and exemptions.	
vi. This certificate is issued as per the provisions given in the Persons with I and its amendment.	Disability Act, 1995
vii. This Certificate is issued for the purpose of his/her admission to (ESE)/M.Tech (EDT) course of NIELIT Aurangabad in the Academi NIELIT Centre, Aurangabad(MS).	
Date:	
Place:	
	Director ORDean /Civil Surgeon

Seal of Institution/Hospital

ANNEXURE X

Physical Fitness Certificate (format)

(To be issued by a Registered Medical Practitioner)

GENERAL EXPECTATIONS

Candidates should have good general physique. In particular,

- a Chest measurement should not be less than 70cm, with satisfactory limits of expansion and contraction.
- b Vision should be normal. In case of defective vision, it should be corrected to 6/9 in both eyes or 6/6 in the better eye. Colour blind and uniocular persons are restricted from admission.
- c Hearing should be normal. Defective hearing should be corrected.
- d Heart and lungs should not have any abnormality and there should be no history of mental illness and epilepticfits.

illness and epilepticfits.									
Name of the cand	Name of the candidate:								
Identification Ma	rk (a n	nole, sca	r or birt	thmark), if	any				
Major illness/ope	ration,	if any (s	specify	nature of i	llness	operation)			
Height in cm:			We	ight in kg:			Blood	Gı	roup:
Past History		Mentali Epilepti							
Chest			(a) Ins	spiration in	ı cm		(b) Expi	rati	ion in cm
Hearing									
Vision withor without glasses:	R	ght Eye	;	Left Eye		Colour Bl	indness		Uniocular vision
Respiratory Syste	m								
Nervous System									
Heart			a) S	ounds			b) Mu	rm	ur
Abdomen			Her	nia			Hydrocele		
Liver Spleen									
Any other defects	:								
Certificate of M	Certificate of Medical Fitness (tick appropriate box below)								
The candidate fulfils the prescribed standard physical fitness, medical fitness and is fit for admission to DEPM/B.Tech/M.Tech course of NIELIT Aurangabad.									
The candidate does not fulfill the prescribed standard of physical fitness/medical fitness and is									
unfit/temporarily unfit for admission due to following defects:									
Name of the Doct	or	Signat	ure with	n date	Regi	istration nu	mber	Se	eal

ANNEXURE XI

Sponsorship Certificate

(On letterhead of the Institute /Organization)

Outward No.:	Date:_
To,	
The Dean Academics, NIELIT Aurangabad Dr. B A M University Campus, Aurangabad 431 004	
This is to certify that Mr. / Ms	is serving in ince
The Organization / Institution has no objection for the mentione at NIELIT, Aurangabad and will permit the candidate to attend le	
The Organization / Institution will render all possible help to him	/ her in persuasion of studies.
He / She will be relieved for a requisite period, if selected for the	course.
Signature of Competent Authority	
Name: Designation:	
Seal of Sponsoring Organization	

ANNEXURE XII

No Objection Certificate For M.Tech (EDT) Part Time Candidate (On letterhead of the Institute /Organization)

Outward No.:	Date:_
To, The Dean Academics, NIELIT Aurang Dr. B A M University Campus, Aurang	
This is to certify that Mr. / Msour Organization / Institution as	is serving insince
The Organization / Institution has no ob Part time Course at NIELIT, Aurangabac	ojection for the mentioned candidate to join the M.Tech (EDT) d.
The Organization / Institution will rende	r all possible help to him / her in persuasion of studies.
He/ She will be relieved for a requisite p	eriod, if selected for the course.
© 1	n distance from the institute. If candidate resigns or transferred in this regard will be given to your office in writing within a
	Signature of Competent Authority
	Name: Designation:
	Seal



NIELIT AURANGABAD **IN NEWS PAPERS**

'नाईलीट' में आईआईटी स्तर प्राप्त करने की क्षमता : गुप्ता

संस्था का स्थापना दिवस मना उत्साह में बाद । २२ सितंबर। लोस सेवा

हाँ याचासाइय अधिडकर माराठ्याहा परिसर स्थित नेत्रनल इन्टरिट्यूट ऑफ इलेक्ट्रिनिक्स एंड एंक्रारिट्यूट टेक्नोलार्गित (नाहिल्ट्टी) संध्या में आईआईटी का स्वर प्राप्त करने की समता है. यह विचार संस्था के कार्यकारी संसालक संतीय कुमार गुप्ता ने क्यांक किए. गाईलीट संस्था की और से हाल ही में देखां क्यांना एक स्वराण एक साथ



Apna Aurangabad Page No. 8 Sep 23, 2019 Powered by: sraken

Union minister Dhotre pays visit to NIELIT

Union minister of sur-for electronics and infor-mation technology Sanjay Dhotre recently visited the National Institute of Electronics and Information Technology (NIELIT). Dr Sanjeev Kumar Gupta (executive director, and in-ternation of the control of the surface of the control of the property of the control of the property of the control of the surface of the control of the control of the police, govern-

union minister of state for electronics and informat technology Sanjay Dhotre during his recent visit to NIELTI. Also seen are Dr Sanjeev Kumar Gupta (executive director, NIELTI) and Marathwada 2evelopment Board chairman Dr Bhaounnia In his speech, Dhotre sai¹⁴



'नाईलीट'मध्ये आयोजित शिबिरात ७० विद्यार्थ्यांचे रक्तदान

Hello Aurangabad Page No. 7 Apr 15, 2019 Powered by: erelego.com

लोकमत समाचार

'नाइलीट' संस्था में विद्यार्थियों के आविष्कारों के दर्शन

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नीलिट'चा औद्योगिक विकासात वाटा

म. टा. प्रतिनिधी, औरंगाबाद

'राष्ट्रीय इलेक्ट्रॉनिक्स आणि माहिती तंत्रज्ञान संस्थेचा (नीलिट) विभागातील शैक्षणिक, औद्योगिक विकासात वाटा आहे. अशा प्रकारची राष्ट्रीय संस्था या क्षेत्राचा भाग असल्याचा अभिमान आहे', असे प्रतिपादन मराठवाडा वैधानिक विकास मंडळाचे अध्यक्ष डॉ. भागवत कराड यांनी संस्थेच्या वर्धापनदिनानिमित्त आयोजित कार्यक्रमात केले.

संस्थेच्या ३२व्या वर्धापनदिनानिमित्त गुरुवारी कार्यंक्रम झाला. यावेळी व्यासपीठावर कार्यकारी संचालक डॉ. संजीवकुमार गुप्ता यांची प्रमुख उपस्थिती होती. यावेळी डॉ. कराड 'संस्थेने मराठवाड्यातील विद्यार्थ्यांना उच्च शिक्षणासाठी प्रेरित माज़ी भूमिका या भागाच्या शैक्षणिक, केले. संस्थेतून विद्यार्थ्यांनी अधिकाधिक ज्ञान संपादित केले पाहिजे. त्यांचे



डॉ. कराड यांचे वर्धापन दिनानिमित प्रतिपादन

व्यक्तिमत्त्व विकसित केले पाहिजे. आरोग्य, औद्योगिक विकासकडे आहे. या संस्थेच्या सर्व आगामी

प्रकल्पांमुळे संस्था अधिक प्रसिद्ध होऊन भारतातील एक सर्वोत्कृष्ट संस्था होईल. आयआयटीचा दर्जा प्राप्त करण्यासारखी या संस्थेची क्षमता आहे. संस्थेच्या विकासासाठी आपण खांद्याला खांदा लावून उभे राहू, संस्थेच्या विकासासाठी सर्वतोपरी सहकार्य करू', असे आश्वासन त्यांनी दिले. संचालक प्रशिक्षणा व्यतिरिक्त इलेक्ट्रॉनिक्स, माहिती तंत्रज्ञानाच्या विविध क्षेत्रातील प्रशिक्षणामध्ये नायलिटचा मुख्यत्वे सहभाग आहे. पब्लिक प्रायक्टेट पार्टनरशिप मॉडेलच्या माध्यमातून संस्था राष्ट्रीय स्तरावर कार्यरत आहे'. याप्रसंगी संस्थेच्या आवारात प्रमुख अतिथींच्या हस्ते वृक्षारोपण करण्यात आले. शशिकुमार गेरा यांनी

डॉ. गुप्ता म्हणाले, 'पोलिस, सशस्त्र सेना, राजकारणी, व्याख्याते तसेच व्यावसायिकांच्या नियमित शैक्षणिक

lokmat Times

Students exhibit talent at NIELIT





Aurangabed First Page No. 5 Mar 15, 2018 Powered by: erelego.com

मा' विद्यार्थ्यांच्या कल्पनांना पंख

'इलेक्रोमा-२०१८'चा पहिला दिवस गाजला, तीन दिवस महोत्सवाची धूम

म. टा. प्रतिनिधी. औरंगावाद

भा टो. आतामधा, आत्रावाम संस्थेअस- राटेअस्पर्सेल स्रोक्षींग स्था असंसे, हिरेल्या संस्थानेस्य सर्किट संदे प्राथ करणे असी सं, यहता 'गेर्स र्रत 'पूना' देशान्त्रसामधा रहना अंत्र अधिकार सुलले ता, क्रिकेट, संस्थर अंदिकार सुलले ता, क्रिकेट, संस्थर अंदिकार सुलले ता, क्रिकेट, संस्थर अंदिकार सुलले ता, क्रिकेट, संस्थर इंट्रमून देशान्या स्थानी 'हलेकीमा-रूट रूट' या प्रतिक दिवस माजला केदीय संगणक च तंत्रसाम संस्थेमध्ये (निल्ट) सुरू सालेल्या उपकासाम मामी अभियासी गाँची केती आहे.

(जिंक्ट) सुरू आनंत्या उपज्याना भागी अर्भारकारी मार्च केता आहे. संग्रेण्या अवकाश १६ सार्चपरी सार्वकार आहे परिवार विकास अहार प्रतिकार अहार प्रतिकार अहार प्रतिकार अहार प्रतिकार अहार प्रतिकार सार्वकार आहे. परिवार का सार्वकार आहे अहार का सार्वकार विकास अहार का सार्वकार विकास अहार का सार्वकार विकास अहार का सार्वकार का सार











टेक्निकलस्पर्धांमधून विद्यार्थ्यांच्या कल्पना समोर येतात, स्पर्धेचे आकर्षण अससे रोवा रेश स्पर्धा, इतर इजिनिअरिंग कोलेजपेक्षा आसी तथार केलेला ट्रॅक अधिक खडनर असतो, त्यामुळे त्याला रिकाराकी स्टान्ट









विद्यार्थ्याच्या संकल्पनेतृत महोत्सव रावविला जातो. टेनिनकल, नांन टेलिनकल अणा विविध उपक्रमांची आखणी करण्यात वेते. तंत्रज्ञानाणी निगडित संकल्पना असतात. विविध जिल्ह्यातृत सर्धक येतात. संजीवकुमार गुप्ता, संजालक, निलीट.





विद्यार्थी सहभागी झाल्या आहेत.