Optimization and Analysis of 6T SRAM using CNFET at 32nm Regime

Conference Paper · February 2016

CITATIONS
0

READS
237

3 authors:

Satish Turkane
PRAVARA RURAL ENGINEERING COLLEGE, LONI, AHMEDNAGAR, MAHARASHTRA
37 PUBLICATIONS **45** CITATIONS
SEE PROFILE

Avinash Pawar
Sardar Vallabhbhai National Institute of Technology
20 PUBLICATIONS **98** CITATIONS
SEE PROFILE

A.K. Kureshi
Vishwabharati Academy's College of Engineering, Sarola-baddi, Jamkhed Raod, A…
47 PUBLICATIONS **150** CITATIONS
SEE PROFILE

IEEE SPONSORED 3rd INTERNATIONAL CONFERENCE ON ELECTRONICS AND COMMUNICATION SYSTEMS (ICECS 2016)

Optimization and Analysis of 6T SRAM using CNFET at 32nm Regime

Satish M Turkane
Research Scholar,
Department of E &TC,
Matoshri College of Engineering & Research Centre, Nashik.
Savitribai Phule Pune University, Pune, Maharashtra, India.
Email: satish_turkane@yahoo.co.in

Avinash S Pawar
Department of E & TC,
Pravara Rural Engineering College, Loni,
Savitribai Phule Pune University, Pune, Maharashtra, India.
Email: pawar.avinash0007@gmail.com

A K Kureshi
Principal,
Vishwabharti Academy's
College of Engineering, Ahmednagar.
Savitribai Phule Pune University, Pune, Maharashtra, India
Email: akkureshi@rediffmail.com

***Abstract*— As the technology is moving towards nano-scale regime, CNFET is having high stability, high performance and low power dissipation. This makes CNFET a promising device for designing of memory arrays. We have optimized a design of 6T SRAM cell based on 32nm CNFET technology and compared it with MOSFET at same regime. SRAM cell designed by CNFET shows improvement in the SNM for read and write operation. We had examined the read and write operation and obtained the results showing improved performance by using different transistor ratio of small in size. As per the property of CNFET having cell ratio of 2 and pull up ratio of 0.4, there had been improvement in stability, performance and sensitivity on process variation. High SNM is achieved with low nanotube diameter for the SRAM cell. All the simulation is done on HSPICE simulation software using 32nm CNFET Stanford model. Devices and circuits development of low power circuits based on its unique tunneling properties and chirality can further be explored.**

Index Term — Six-transistor static random access memory(6T SRAM), carbon nanotube field effect transistor(CNFET), static noise margin (SNM), cell ratios (CR), silicon on chip (SOC), Pull up ratio (PR).

I. INTRODUCTION

Static Random Access Memories (SRAMs) continue to be very important parts/pieces across wide range of microelectronics applications from consumer wireless to high performance server processors, (combining video, sound, words and pictures together) and System on Chip (SoC) applications[1,14]. For SRAM scaling, difficulties embody maintaining each acceptable noise margins within the presence of accelerating random Green Mountain State fluctuations and random telegraph noise, and dominant instability, particularly hot-electron instability and negative bias temperature instability (NBTI). There square measure tough problems with keeping the outpouring current among tolerable targets, yet as tough lithography and print method problems with scaling. Determination this SRAM challenge is crucial to system performance, since SRAM is often used for quick, on-chip memory [17]. As semiconductor material feature size scales all the way down to the nanometer range, planner bulk CMOS style and fabrication encounter vital challenges [2]. CNTFETs are recognized as a promising candidate for future nano-electronic devices. An exceptional electrical property like high speed, high-K compatibility, and chemical stability has provided CNFETs with wonderful characteristics that match or could exceed those of the state of the art Si based MOSFETs [3]. In addition to the electrical properties CNFETs are less sensitive to several method parameter variations compared to standard MOSFETs [3-4]. Recently, varied authors planned a brand new SRAM Cell style based on CNFETs. This paper proposes to improvement of the assorted parameters of the CNTFET based SRAM Cell with minimum attainable space and delay trade off. In Section II the brief of CNFET is mentioned, in section III the design of static random access memory is specified. The simulation results of MOSFET and CNFET based inverter are compared; also the CNFET SRAM results are mentioned in terms of SNM, Pull Up Ratio, Supply Vdd and Temperature in Section IV. The comparisons of the results are made in Section V with the conclusion. The future scope of work is specified in Section VI.

II. CNFET

A CNTFET refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure [5].

A. Structure of carbon nano tubes

Since the invention of carbon nanotubes (CNTs) by lijimain 1991 [6,13], planer CNTFETs as shown in Figure 1 represent the bulk of devices fabricated to date, principally attributable to their relative simplicity and moderate compatibility with prevailing manufacturing technologies. The coaxial geometry as shown in Figure 2 specifies maximizes the electrical phenomenon coupling between the gate conductor and therefore the carbon nanotube surface thereby causes a lot of channel charge at a given bias then the alternative geometries. This improved coupling is fascinating in mitigating the short-channel effects that plague technologies like CMOS as they downside device options. Parameters such as pitch, channel length (Lch), gate width (W gate), and number of tubes will affect the performance of CNFET. The threshold voltage of CNFET is determined by the CNT diameter [7].

978-1-4673-7832-1/16/$31.00©2016 IEEE

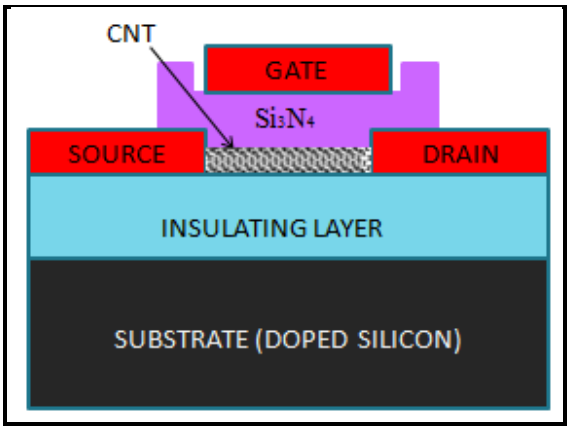

Figure 1: Structures of CNTFETs planar.

The structure of any carbon nanotube can be described by an index with a pair of integers (n, m) that define its chiral vector. In terms of the integers (n, m), the nanotube diameter and the chiral angle are given by [7]

$$d = \frac{\sqrt{3}a\sqrt{m^2+mn+n^2}}{\pi} \quad (1)$$

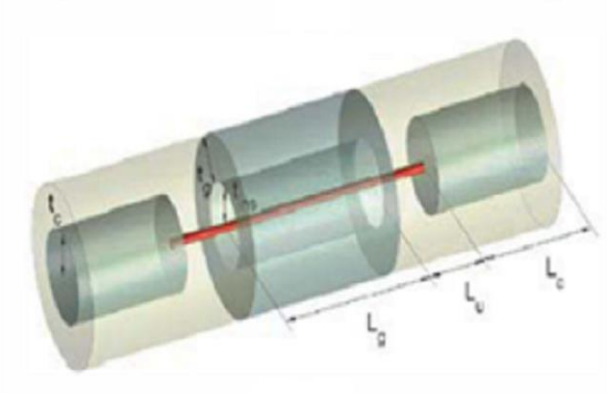

Figure 2: Structures of CNTFET coaxial [7].

$$\theta = \tan^{-1}\frac{\sqrt{3}n}{2m+n} \quad (2)$$

Where a = 0.249 nm is the carbon to carbon atom distance.

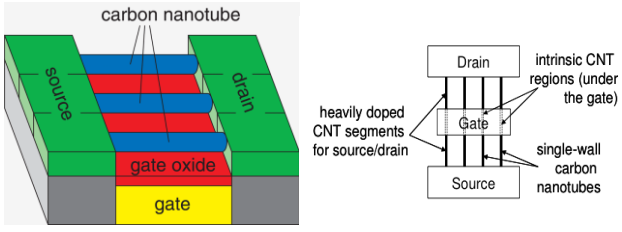

Figure 3: CNFET Structure [3, 8].

III. STATIC RANDOM ACCESS MEMORY

A. Construction of SRAM

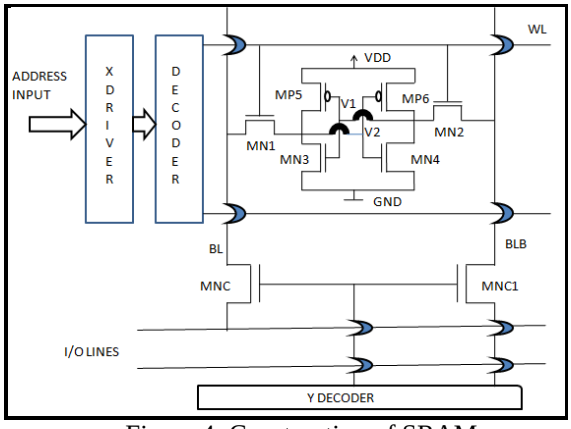

Figure 4: Construction of SRAM.

We have different row and column in between this rows and column there is memory cell having two pass transistors and two cross coupled CMOS inverter. Depending on the x address input one of the address lines goes high and selects the pass transistor in that particular row and that particular cell is connected to BL line and another end is connected to the BLB line. To select one of the column there is again to pass transistor also have their two I/O lines pass transistor in connected to I/O lines. The input from this pass transistor comes from the Y decoder which receives the Y address input and output are pass to the gate of the pass transistor . So depending on the combination at the input Y decoder one of the output of Y decoder is going to high so it basically select one particular column only the output of one particular column is connected to the I/O lines as shown in Figure 4.

Depending on the input address one row will select and with the help of Y decoder we selecting one particular column that column is available on I/O lines. Depending on the combination of X and Y inputs one particular cell will be selected. MNC & MNC1 is access transistor for the column selection [9].

B. 6T SRAM Cell

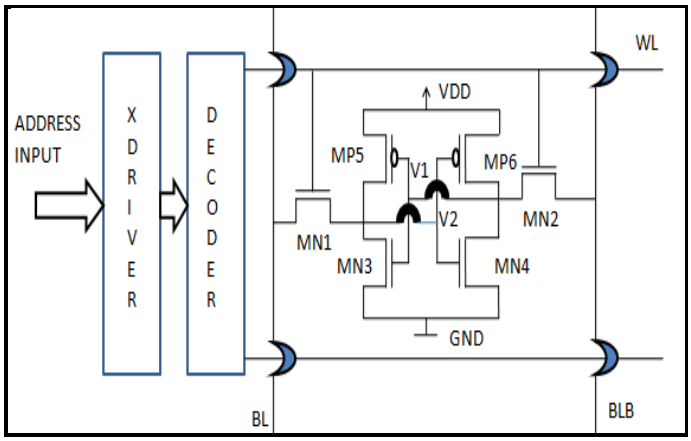

Figure 5: 6T SRAM Cell.

Two cross coupled inverter having transistor inverter 1 (MP5-PMOS & MN3-NMOS) inverter 2 (MP6-PMOS & MN4-NMOS) and two access transistor MN1 (NMOS) and MN2 (NMOS) these transistor enable access to the cell during read and write operation. When world line is activating the two access transistor MN3 and MN4 are connected to the internal node of the cell to the BL and BLB line [16].

TABLE I: Operation of the 6T SRAM.

	Read	Write	Hold
BL	Logic 1	Logic 0	Logic 0
BLB	Logic 1	Logic 1	Logic 0
WL	Logic 1	Logic 1	Logic 0

C. Read Operation

During scan operation WL is activated and also the BL is pre charge to VDD and BLB is store to zero. [10] The voltage at BL is remaining at the pre charge level and also the voltage at BLB discharges through MN2 serial with MN4 electronic transistor.

D. Write Operation

During the write operation, the bit-lines are driven to complementary voltage levels via a write driver then the word-line is chosen [15]. On the facet of the cell that the bit-line voltage is logic '0' (i.e., an occasional voltage), the interior storage node is discharged through the access electronic transistor [11].

E. Pull up and Cell ratio

1) **Pull up ratio (PR):** It is ratio of PMOS of the inverter to the MN1 access transistor right side

$$PR = \frac{W_6 L_2}{L_6 W_2} \quad (3)$$

2) **Cell up ratio (CR):** It is ratio of the NMOS of the inverter and the access transistor MN2 right side

$$CR = \frac{W_3 L_1}{L_3 W_1} \quad (4)$$

Proper W/L ratio is to be design for getting good stability in all modes (read, write, hold).

IV. SIMULATION RESULTS

Select a proper transistor and improve the parameters of the SRAM cell is which plays a major role in designing a SRAM. So we first check the performance of the inverter on CMOS and CNFET and obtain the results. All the simulation is done in the HSPICE software.

A. MOSFET Inverter

Using 32nm CMOS technology we have simulate the CMOS INVERTER output and obtain the following waveform.

TABLE II: Output Voltage of the CMOS inverter.

INPUT VOLTAGE	OUTPUT VOLTAGE
0.00V	2.22V
3.00V	0.01V

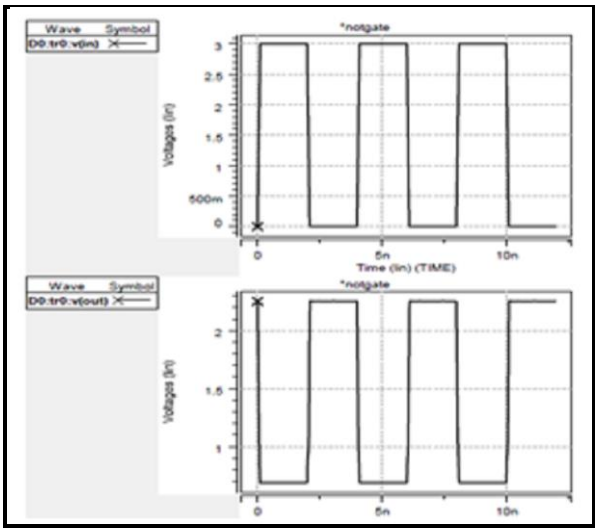

Figure.6: CMOS inverter output waveform.

B. CNFET Inverter

Using CNFET we have simulate the inverter in the HSPICE to obtain the better result than the TFET transistor output and obtain the following waveform.

TABLE III: Output Voltage of the CNFET inverter.

INPUT VOLTAGE	OUTPUT VOLTAGE
0.00V	2.22V
3.00V	0.01V

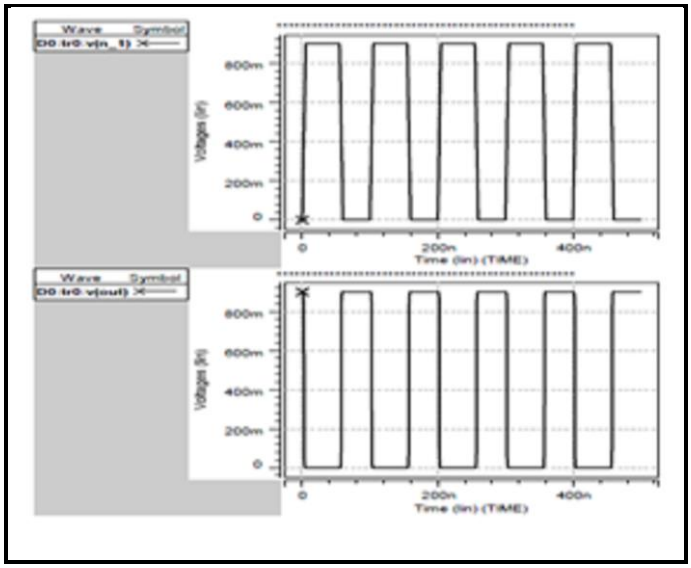

Figure 7: CNFET inverter output waveform.

C. Comparasion and analysis of the CMOS and CNFET inverter

TABLE IV: Comparison of CNFET and CMOS inverter.

APPLIED VOLTAGE	MOSFET	CNFET
0.00V	2.22V	3.00V
3.00V	0.01V	0.00V

D. CNFET simulation of SRAM

The Transistors required for design of a 6T SRAM cell is required to be selected such that it improve the various performance parameters. After selection of proper transistor, sizing plays a important role in the improvement of the SRAM parameters such as small area, low power dissipation, high SNM. Following table shows the transistor sizing and transistor ratio of the CNFET 6T SRAM.

TABLE V: Tube based sizing of CNFET.

Transistor	Number of Tubes
Pull up transistor	2
Pull down transistor	10
Access Transistor	5

TABLE VI: Sizing of the CNFET in SRAM.

Cell Ratio	Pull up Ratio
2	0.4

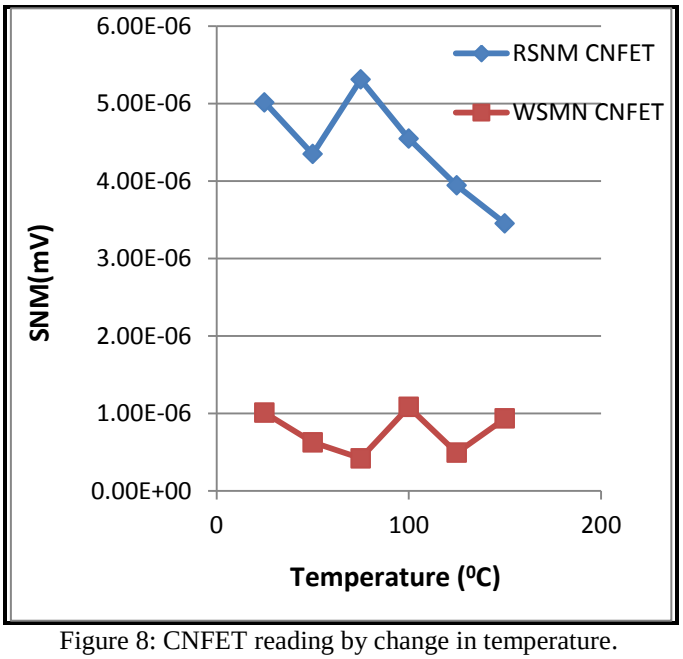

Figure 8: CNFET reading by change in temperature.

Figure 8 shows the various temperatures reading of the CNFET Transistor for design a 6T SRAM cell.

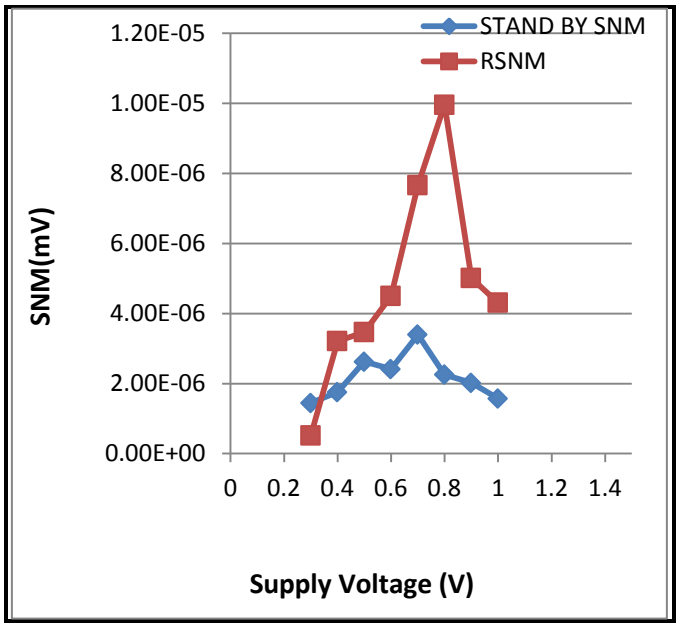

Figure 9: CNFET reading by change in supply voltage.

Figure 9 shows the various supply voltage reading of the CNFET Transistor for design a 6T SRAM cell.

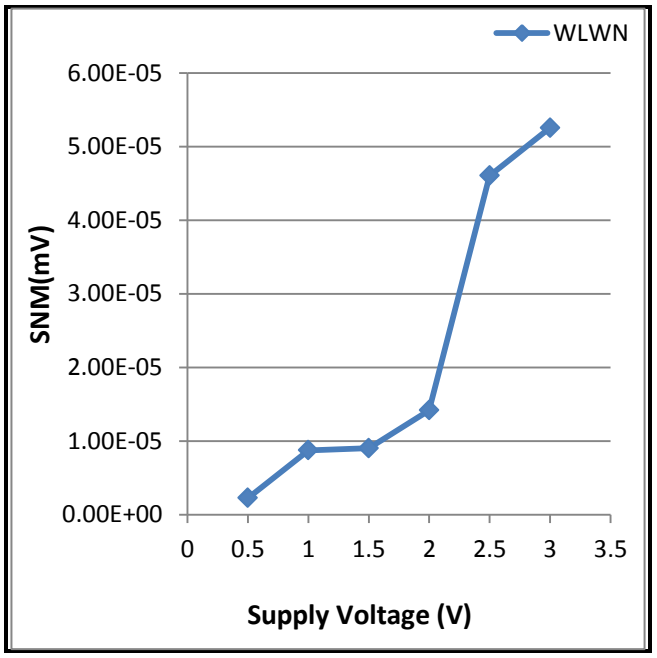

Figure 10: CNFET reading by change in Pull Up ratio.

Figure 10 shows the various reading by change in WL of the CNFET Transistor for design a 6T SRAM cell.

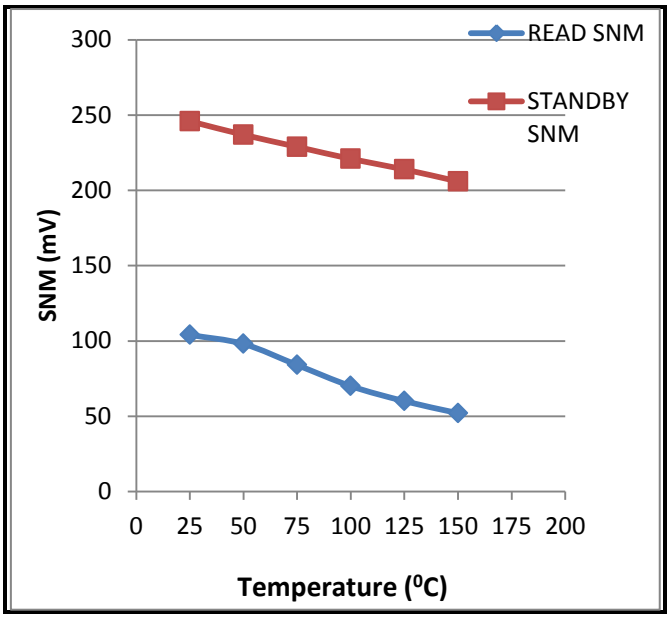

Figure 11: CMOS reading by temperature.

Figure 11 shows the various reading by change in temperature of CMOS Transistor for design a 6T SRAM cell.

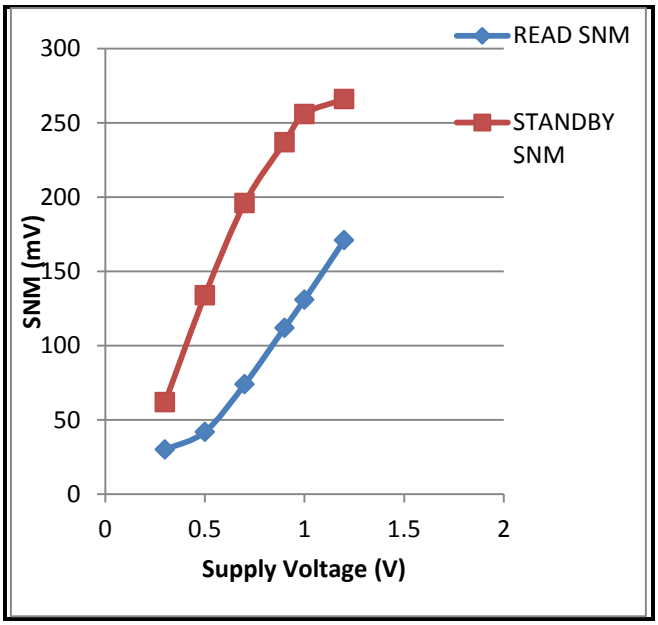

Figure 12: CMOS reading by in supply voltage.

Figure 12 shows the various reading by change in supply voltage of CMOS Transistor for design a 6T SRAM cell.

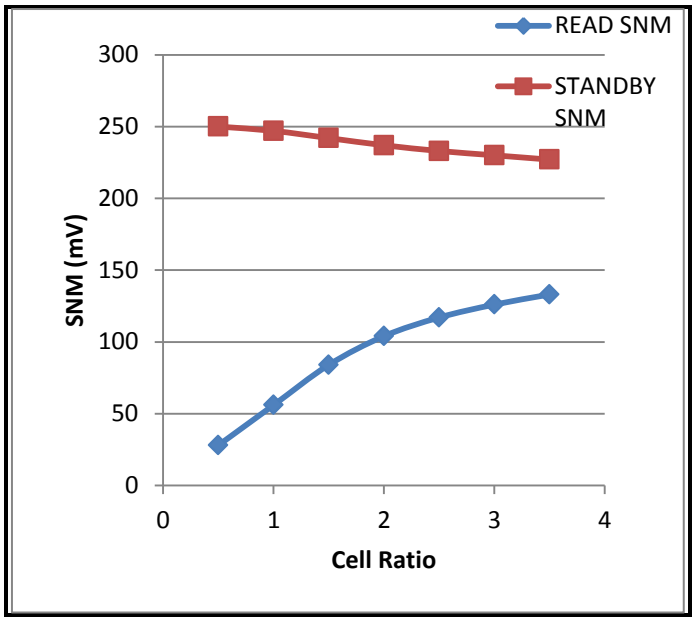

Figure 13: CMOS reading by in cell ratio.

Figure 13 shows the various reading by change in cell ratio CMOS Transistor for design a 6T SRAM cell.

V. CONCLUSION

The CNFET inverter improves the results up to 79% than the conventional CMOS inverter. So we choose the CNFET. Here we have simulate the 6T SRAM in CNFET by comparing the readings of the 6T SRAM MOSFET and CNFET we analysis the read, write and hold maximum cell ratio for read stability and minimum pull up ration for write operation. As per the property of CNFET high supply voltage improves the high stability. The 6T SRAM CNFET having cell ratio of 2 and pull up ratio of 0.4 improve and achieve maximum stability during read operation and also improve the standby mode operation compared with conventional CMOS SRAM.

VI. FUTURE SCOPE

Further analysis within the foresaid space are going to be targeted on growth and placement controlled synthesis of nanotubes of given diameter, chirality. As we scale down the transistor size it will be difficult to drive data line so issue it can be overcome by sense amplifier in memory array. Additionally the areas of CNFET's in terms of conformal deposition of ultrathin high-k dielectrics on nanotubes alongside devices and circuits development of low power circuits supported its distinctive tunneling properties are often explored.

REFERENCES

[1] Jawar Singh and Balwinder Raj, "SRAM Cells for Embedded Systems", ET Docket,ISBN 978-953-51-0167-3, InTech, pp. 388-406, March 02, 2012.

[2] Yu-Ming Lin, J. Knoch, Ph. Avouris,"High performance carbon nanotube field-effect transistor with tunable polarities," IEEE Transactions on Nanotechnology., Vol. 4, pp. 481-489, September, 2005.

[3] J.Appenzeller, "Carbon Nanotubes for High-Performance ElectronicsProgress and Prospect," Proceedingsof IEEE, Vol. 96 Issue. 2, pp. 201 -211, February, 2008.

[4] S. Lin, Y.B. Kim, F. Lombardi, and Y.1. Lee, "A New SRAM Cell DesignUsing CNTFETs," Proceedings of IEEE International SoC Conference, pp. 168 -171, November, 2008.

[5] T. Dang, I. Anghel, and R. Leveugle, "CNTFET Basics and Simulation," IEEE International conference on Design and Test of Integrated Systems inNanoscale Technology (DTIS), Tunis, Tunisia, pp. 28-33, September, 5-7, 2006.

[6] Sumio lijima, "Helical microtubules of graphitic carbon nature," Nature, International weekly Journal of Science, *Nature*, pp. 56 – 58, November, 7, 1991.

[7] G. Timp,"Nanotechnology," Springer-Verlag, New York, First Edition, pp.309-310, 1998.

[8] Stanford University CNFET Model Web site. (2008).Available: http://nano.stan ford.edu/model. phpid=23.

[9] http://www.nptel.ac.in/courses/117101058/downloads/Lec-28.pdf.

[10] Changhwan Shin, Min Hee Cho, YasumasaTsukmoto, Bich-Yen Nguyen,Carlos Mazure, Borivoje Nikolic and Tsu-Jae King Liu "Performance andArea Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells atthe 22-nm Node," IEEE Transactions on Electron Devices,Vol. 57, No 6, pp. 1301-1309, June, 2010.

[11] Hossein Aghababa1, Behzad Ebrahimi1, Ali Afzali-Kusha1,and MassoudPedram, "Probability Calculation of Read Failures in Nano-ScaledSRAM Cells under Process Variations," Journal of Microelectronics Reliability, Vol. 52, Issue. 11, pp.2805-2811, November, 2012.

[12] A.K.Kureshi , Mohammad Hasan, "Performance comparison of CNFETand CMOS-based 6T SRAM cell in deep submicron," Journal of Microelectronics, Volume 40, Issue 6, pp.979-982, June, 2009.

[13] Rajendra Prasad, S.B.K.Madhavi, and K Lal Kishore, " Design of 32nm Forced Stack CNFET SRAM Cell for leakage power reduction," 2012 International Confernce om Computing Electronics and Electrical Technologies (ICCEET), 2012.

[14] S Rajendra Prasad," Desgn of 32nm 7T SRAM Cell based on CNFET for low power operation," 2012 International Conference on Devices and Systems (ICDCS), 2012.

[15] Chopade.S.S., and D.V.Padole, "Stability analysis of 6T SRAM cell for nano scale FD-SOI technology," 2014 Annual IEEE India Conference (INDICON), 2014.

[16] Zhang, Zhe, Micheal A. Turi and Jose G. Delgado-Frias., "SRAM leakage in CMOS, FinFET and CNFET technologies: leakage in 8t and 6t sram Cells," Proceedings of the great lakes symposium om VLSI-GLSVLSI 12, 2012.

[17] 2013 Edition-ITRS. Availiable online at: www.itrs.net/ITRS%20199.../2013ITRS/2013Chapters/2013PIDS_Sum.