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DESIGN LOW VOLTAGE CURRENT MIRROR AT 32NM REGIME

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***Abstract*: As the technology moving towards lower voltage for high stability and accurate performance. We design low voltage current mirror using IGFET, FDSOI, CNTFET.These transistor is moving towards low-voltage high-speed performance. Here in this paper, we have design low voltage current mirror for Accurate duplication of current. To obtain accurate duplication of current, we verify the performance of low voltage current mirror on FDSOI and CNTFET Transistor having the 32nm technology. The circuit is simulated with 32nm technology for FDSOI and CNTFET. They operate at lower power supply than IGFET. The simulation results show the improvement in knee voltage 1.7v and 1.3v for the current mirror.**

Keywords— Carbon nanotube field- effect transistor (CNTFET); Fully *Depleted Silicon on Insulator (FDSOI)*; Insulated Gate filed effect transistor (IGFET).

I. INTRODUCTION

Nowadays technology is moving towards the nanoscale for the evolution of high-speed computers and upgraded communication devices. Additional chips have low size; minimum power is required [1] So for gaining less power and minimum voltage we have to double the size of transistor every 18 months [2]. Current mirror fundamental fabric for nearly all continuous circuits confirm shows the analog structures thatfor the most part determine by their fractures. For small scale voltage style circuit, small scale voltage currents mirrors area unitobligatory with high performance. The current mirror correctness and result resistivity are the first necessary guideline to dictate the performance of this mirror. The application like high speed, the sinking time of current mirror is important parameter [3] [4] [5]. Hence voltage scaling was introduced as an effective way to lower the energy consumption. It can be observed that minimal energy can be achieved by reducing the supply voltage below the threshold value, but it deteriorates the system performance. Near threshold, an operation is considered to provide better results regarding optimized values of power consumption and performance. [6-7] the new technology transistor FDSOI and CNFET are used for low power combustion and high performance. The FDSOI and CNFET operation will be described in section II and III. All experimental results and theory we describe in section V &IV.

II. FDSOI DEVICE

In typical bulk Si microcircuits, the active components are placed during a thin surface layer and are far away from the Si substrate with a reduction in some layer of a contact. The discharge current of this connection will increase as expressed by a mathematical exponent with temperature and is to blame for many serious dependableness issues. We say that the effect of the small in scale orbits is restricted by this desirable discharge current and peak power dissolution at high temperatures. So, augmented request for an extremist low power, rapid circuits is pushing the gadget fabrication method travel on the far side submicron technologies that could not be reached with hugeness CMOS method resulting in the alternate, Si movement stuff silicon on insulator technology [12]. Si on stuff silicon on insulator technology employs skinny parts of Si substrate by a comparatively thick layer of oxide. The SOI scientific knowledge dielectrically separates parts and additionally with towards separation, become smaller numerous parasitic capacitances and so completely remove the chance of latch-up failures. Silicon on insulator technology conjointly defines producing method by excluding with skill and field execution footsteps and permits small fabrication, more volume, and quicker small-scale circuits, with less in the amount a device used to connect two things together unwanted transfer of the signal between communication channel. These options create silicon on insulator technology extraordinarily engaging in rising on-chip system small scale circuits, small denoting a mechanical device which eclectically operates like (MEMS) and homogenous for optical component applications. Our prior attention is entirely focused on depleted (FD) structure as an outcome belong to benefits above the part evacuate model,

like (1) FD-SOI appliances are without appropriate intervention complimentary from kink impact, also have the best improvement in circuit speed, consume less power needs and maximum level of soppy error release. FD appliances carry out quicker attributable to a beguiler sub approaches for slope and a reduced approach to a voltage that enables for the more immediate shift of the CMOS. These transistors even have augmented currents at various low voltages. Metallic element fabric to be subjected from the transient body impact that successively adds to the History impact [13, 14].

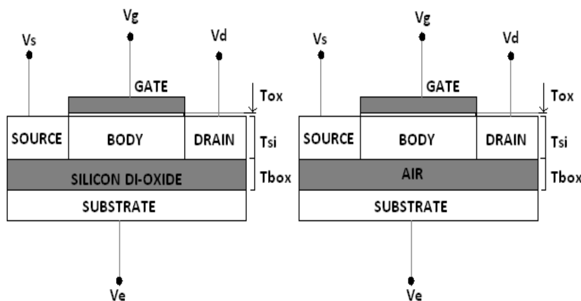

Figure. 1. Cross-sectional structure of a) FDSOI b) FDSONs

III. CNTFET DEVICE

The Material single wall CNT and Multi-wall CNT is utilized to design CNTFET as the channel material instead of bulk silicon in the traditional MOSFET structure [9]. A CNT could be a rolled tube of Carbon atoms during a honeycomb arrangement. This device having three terminal including nanotube conducts in between the source and drain terminal, and behavior like a shipper channel, that is either activated or deactivated through the gate terminal. Various types of CNTFET have been fabricated, Schottky-barrier CNTFET, partially-gated CNTFET and doped-S/D CNTFET [10] Planar CNTFETs as shown in Figure l represent the bulk of devices invented thus far, largely as a result of their relative simplicity and moderate compatibility with existing producing technologies. The better pairing is fascinating in the reduction of short-channel effects that beset the technologies like CMOS as CMOS having disadvantages, so we have CNFET device in option. The performance of CNFET is improving due to the parameters like pitch, the channel length (Lch), gate size (W gate), also many of tubes. The edge voltage of CNFET is decided by the CNT diameter [11]. Within the fabrications steps of the CNFET contact resistance square measure come back.

IV. CURRENT MIRROR

The primary current mirror implemented mistreatment MOSFET transistors is as shown in Figure 3. Here we've got an inclination to assume that every transistor pecuniary resource and pecuniary resource working in saturation or active region. Throughout this circuit, there is a directly proportional to IREF and IOUT.

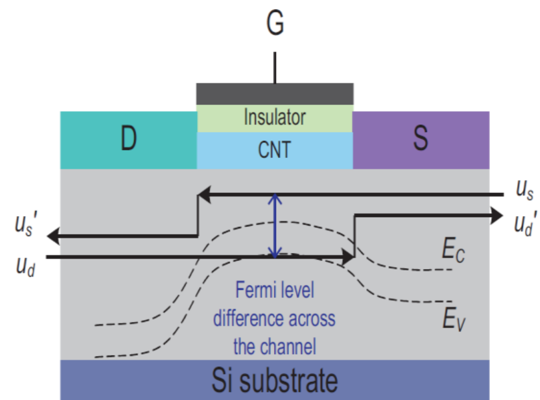

Figure. 2. Ideal CNFET with ballistic channel [8]

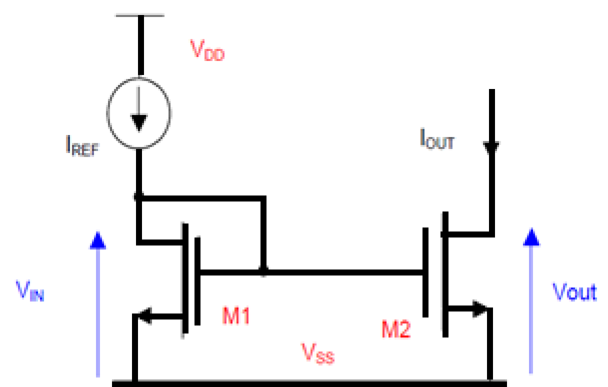

Figure 3. Basic Current Mirror

The ID of a MOSFET DRAIN is set not solely through VGS terminals however conjointly the drain-to-gate voltage of the MOSFET. So the drain current often states as

$$ID = f(VGS, VDG).$$

This relationship can be from the MOSFET device.

$$VDS=VDG+VGS.$$

With this substitution, it is an approximate form for function f (VGS, VDG):

$$Id = f(VGS,VDS) = 0.5\ Kp()\ (VGS - Vth)2(1 + \lambda VDS)$$

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$$Id= 0.5\ Kp()\ (VGS - Vth)2(1 + \lambda(VDG+ VGS))[15]$$

Here Kp of the transistors depends on the technology of fabrication, W/L of the transistor, VGS, VTH, and VDS voltages respectively, λ is the channel length modulation constant of the transistors.

Now from the figure 3 we can write for M1 as the mirror circuit,

$$ID = IREF.$$

Now for the circuit, the supportive current IREF may well be a notable of stable current worth freelance of giving voltage fluctuation. We tend to could use an electrical device as shown, or perhaps a "threshold-referenced" or "self-biased" current supply to produce this stable reference current.

Now because VDG=0 for semiconductor money supply, that the perform for the drain current of money supply are often given by

$$ID = f\ (VGS,\ VDG=0),$$

Thus, IREF depends solely on the VGS. Thus the current IREF states the value of VGS.

Now from circuit, the same VGS is applied to transistor M2. Then M1 and M2 are matched and having the same length of the channel, gate size, VTH voltage and as VDG=0 to M2 as well, then output current IOUT is varies regarding VGS only for M2, so IOUT = IREF. When VDG= 0 for the output transistor and both transistors are matched with identical W/L.

V. SIMULATION RESULTS

Using 32nm technology CMOS, FDSOI and CNTFET transistor we simulate the current mirror circuit and observe the various readings are as given.

Cmos Current Mirror

As technology is scaling up to 32nm, we observe that on the knee voltage at 1.02v we obtain the current mirror as shown in the waveform.

Fdsoi Current Mirror

As technology is scaling up to 32nm FDSOI, we observe that accurate duplication of current is obtain on the knee voltage is slightly larger than the CMOS as shown in the waveform.

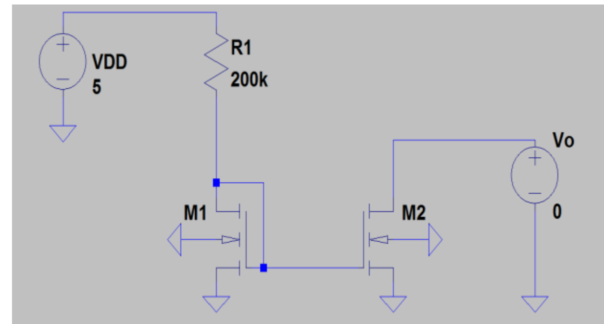

Figure 4. Design of Current mirror for simulation

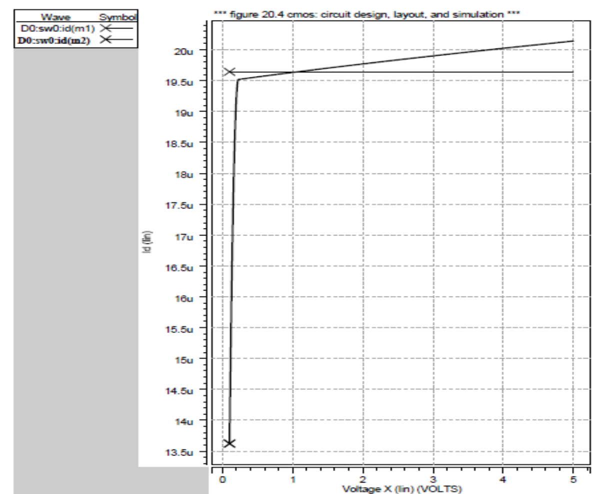

Figure 5. CMOS Current Mirror at 32nm waveform

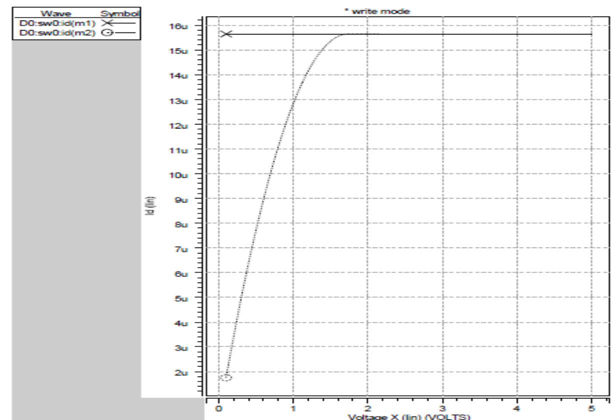

Figure 6. FDSOI Current Mirror at 32nm waveform

The knee voltage 1.7v for the FDSOI from which we obtain the accurate mirror.

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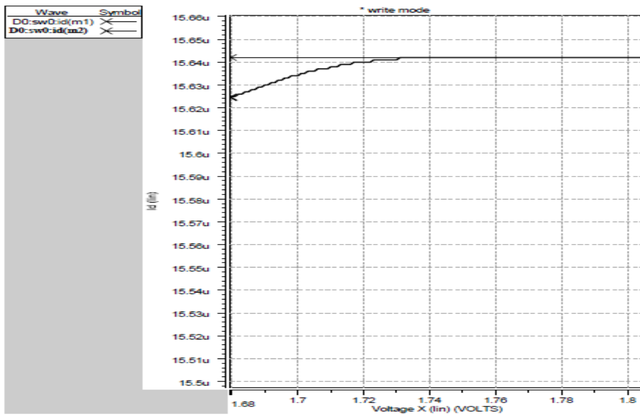

Figure 7. FDSOI Current Mirror knee voltage waveform

CNTFET Current Mirror

As technology is scaling up to 32nm CNTFET, we observe that accurate duplication of current is obtained at knee voltage 1.30v is which is much improved than the FDSOI transistor.

VI. CONCLUSION

The comparative analysis of current mirror at 32nm technology for the various transistor. To obtain the actual duplication current at low voltage CNTFET is a promising device for low voltage current mirror design at 1.3v knee voltages shows the accurate, current mirror as comparing the CMOS, At the same time,FDSOI is also shown the exact duplication of current at 1.7v as compare to CMOS.

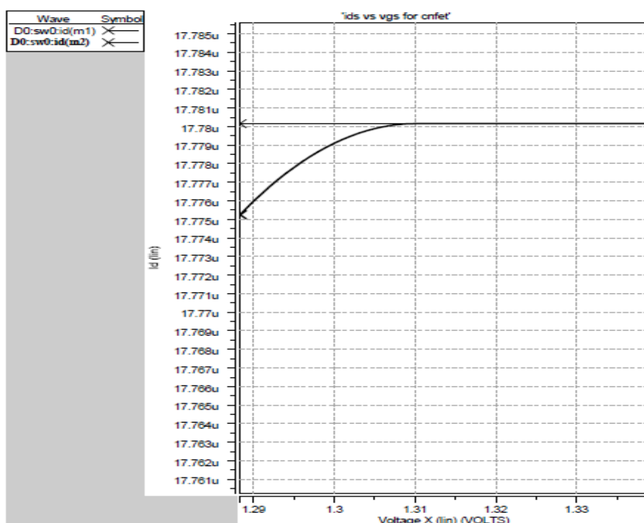

Fig. 8. CNFET Current Mirror knee voltage waveform

TABLE 1 Current Mirror Knee Voltage.

Types of Transistor	Knee Voltage from Mirror starts
FDSOI 32nm	1.73v
CNTFET 32nm	1.30v

VII. FUTURE SCOPE

So the CNTFET is a promising device for design the low voltage current mirror for various applications like ECG. The requirement is knee voltage is more reduces than the obtain results.

REFERENCES

[1]. Minghong Li, H.L. Kwok ''The Application of Current-mode Circuits in the Design of an A/D Converter '' Electrical and Computer Engineering, 1998. IEEE Canadian Conference on, Volume 1, 24-28 May 1998Page(s):41 – 44

[2]. http://nptel.ac.in/courses/106104024/2

[3]. Kuo-Hsing Cheng, Chi-Che Chen and Chun-Fu Chung ''AccurateCurrent Mirror with High Output Impedance'' Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference, Volume 2, 2-5 Sept. 2001 Page(s):565 – 568

[4]. Kuo-Hsing Cheng', Tsung-Shen Chen2, and Ching-Wen Kuo ''High accuracy current mirror with low settling time'' Circuits and Systems, 2003. MWSCAS '03. Proceedings of the 46th IEEE International Midwest Symposium, Volume 1, 27-30 Dec. 2003 Page(s):189 – 192 Vol. 1

[5]. MilindSubhashSawant, Jaime Ramirez-Angulo, Antonio. J. Lopez- Martin and Ramon G. Carvajal '' New compact implementation of a very high-performance CMOS current mirror" circuits and systems, 2005.48th Midwest Symposium, 7-10 Aug. 2005 pp. 840-842

[6]. D. Markovic, C.C.Wang, L.P.Alarcon, T.-T.Liu, J.M.Rabaey, "Ultra low- power design in near-threshold region," Proc. IEEE, Vol. 98, no. 2, pp. 237–252, 2010.

[7]. S. Chandra, A. Raghunathan, S. Dey, "Variation-aware voltage level selection," IEEE Trans.VLSISyst, Vol. 20, no. 5 pp. 925–936, 2012.

[8]. Jie Deng and H.-S.Philip Wong. A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its application - part i: a

model of the intrinsic channel region. IEEE Transactions on Electron Devices, 54:3186–3194, 2007.

[9]. T. Dang, I. Anghel, and R. leveugle, " CNTFET Basics and Simulation," IEEE International Conference on Design and Test of Integrated Systems in Nanoscale Technology (DTIS), Tunis, Tunisia, pp. 28-33, September 5-7, 2006.

[10]. J. Guo, S. Datta, M. Lundstrom, "Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors," *IEDM*, pp. 711-715, 2002.

[11]. Appenzeller "Carbon Nanotubes for High-Performance ElectronicsProgress and Prospect," Proc. IEEE, Volume 96, Issue 2, pp. 201 - 211, Feb. 2008.

[12]. COLINGE J P. "Silicon on insulator technology: Materials to VLSI." 2nd ed. Norwell, MA: Kluwer: Kluwer Academic Publishers; 1997.

[13]. Guegan, G., Gwoziecki, R., Touret, P., Raynaud, C., Deleonibus, S., Pretet, J., Gonnard, O., Gouget, G., "New floating-body effect in partially depleted SOI pMOSFET due to the direct tunneling current in the partial n+ poly gate", Solid-State Device Research Conference, 2008. ESSDERC 2008. 38th European, On page(s): 59 – 62.

[14]. Mercha, A., Rafi, J.M., Simoen, E., Augendre, E., Claeys, C., "Linear kink effect induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETS", Electron Devices, IEEE Transactions on, On page(s): 1675 - 1682 Volume: 50, Issue: 7, July 2003.

[15]. BehzadRazavi, Design of CMOS Analog Integrated Ckts, Mc-Graw Hill College, 2001.