NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY AURANGABAD

राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान ,औरंगाबाद

Ministry of Electronics & Information Technology

Government of India

CERTIFICATE COURSE IN VLSI DESIGN

OBJECTIVE

This Course in VLSI Design provides a broad working knowledge in **Digital IC Design and Verification**. Better understanding of VHDL and Verilog coding and documentation provides best practices on FPGA/CPLD architecture, and the ability to read and interpret existing code.

The main **Objective** of this course are :

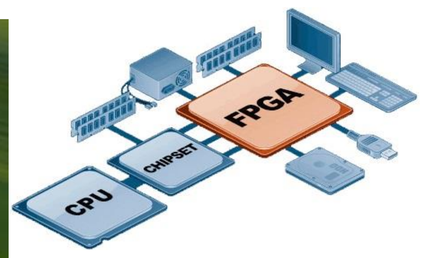
- Designing of Digital Circuit
- Analyze HDL Coding Logic Design and Synthesis
- FPGA prototyping

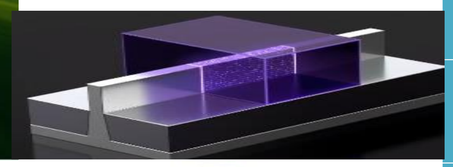
ELIGIBILTY

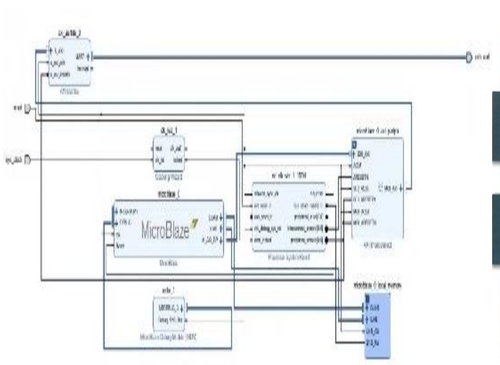
Diploma, BE / B.Tech., ME / M.Tech., BCA / MCA, M.Sc./ B.Sc in (IT/CS/Electronics/Electrical/Instrumentation) or equivalent of any of these.

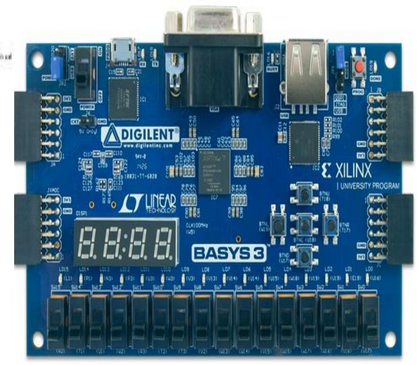
DURATION

Duration: 50 Hours









Sr. No.	Course Content
1	Introduction to VHDL
2	Introduction to Verilog
3	Detail modeling styles in VHDL
4	Detail modeling styles in Verilog
5	Introduction to ASIC and FPGA design flow
6	Introduction to Combinational circuits and its examples
7	Introduction to Sequential circuits and its examples
8	Introduction to FSM circuits and its examples
9	Introduction to Vivado
10	Project creation in Vivado
11	Project simulation and test bench verification in Vivado
12	Project synthesis as per the examples
13	Synthesis of Combination logic with examples
14	Synthesis of Sequential logic with examples
15	Synthesis of FSM with examples
16	How to create IP in Vivado
17	Use of existing IP in Vivado
18	Create Softcore processor IP
19	Demo examples using Basys-3 board
20	Completion of Mini Project

Certificate

Certificate will be provided to the participants, based on minimum 75% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

Training Calendar:

Expected Date of Batch starts from 20th December 2021

Registration and Fee Details

For Registration/Course fee

Rs. 4,100/-

CLICK HERE

*Course will be delivered in Online Mode

Bank Account Details

Name	NIELIT AURANGABAD
Bank Name:	Bank of Maharashtra
IFSC Code:	MAHB0000152
Account Number:	20060526862
Branch:	University Branch

Contact Person

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CLICK HERE For Registration

National Institute of Electronics & Information Technology Aurangabad
CEDTI Complex, Dr. B.A.M. University campus
Aurangabad, Maharashtra-431004
http://www.nielit.gov.in/aurangabad/

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Online Certificate Course in VLSI Design

Course Duration - 50 Hours **Total - 2 Hrs. per Day**

Theory-1Hr. & Lab-1 Hr.

Course Description:

- Hardware Modeling Overview.
- VHDL & Verilog language concepts.
- Test benches Writing.
- Coding for Synthesis.
- FPGA Architecture - Basic Components of FPGA (LUT, CLB, Switch Matrix, IOB).
- FPGA Architecture of different families: Artix-7 FPGA and Basys-3 Board.
- FPGA Design Flow - Xilinx Vivado tool, Reading Reports, SSN and Implementing IP cores, soft-core processor IP Design using MicroBlez.
- Optimal FPGA Design - HDL Coding Techniques for FPGA, FPGA Design Techniques.
- Synthesis Techniques, Implementation Options.

Eligibility:

- Diploma/B.Sc./M.Sc./B.Tech./M.Tech. in Electronics/Electrical/Science stream/ Instrumentation (Completed or Pursuing).

Prerequisite:

- Basic Knowledge of Analog & Digital circuits.

Fee & Important dates:

Last Date for Registration & Payment	Expected Date of Course Start	Course Fee
19/12/2021 {Sunday}	20/12/2021 {Monday}	Rs. 4,100/- incl. GST & all other charges

Mode of Course Delivery:

The course would be conducted in virtual classroom environment which will be completely online, Course content includes Online Theory & lab sessions, Live interactive doubt clearance sessions, Course material in text/pdf format, Links to external resources and blogs, Online Forums, Lab Assignments, Tests etc.

Certificate:

Certificate will be provided to the participants, based on minimum 75% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

How to Apply:

- Read the course structure & course requirements carefully.
- Visit the Registration portal and click on apply button.
- Create your login credentials, fill up all the required details, check preview and Submit the application form.
- Login with your credentials to verify the mobile number, email ID and then upload the documents, Lock the profile and Pay the Fees online, using ATM-Debit Card / Credit Card / Internet Banking / UPI etc.

Contact Person:

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Course Content

Theory Topics	Hours	Practical/Lab Assignments	Hours
➢ Introduction to VHDL 1. Basic Concepts 2. Introduction to modeling's 3. VHDL Data Types	6 Hrs	➔ How to download and Install Vivado Software ➔ Install web pack License on Vivado	1 Hrs
➢ Introduction to Verilog	1 Hrs	➔ How to create Project in Vivado with example	2 Hrs
➢ Detail modeling's of Verilog 1. Behavioral modeling 2. Data flow modeling 3. Gate level modeling 4. Switch level modeling	4 Hrs	➔ How to write Test bench waveform with example	2 Hrs
➢ Introduction to ASIC and FPGA-FPGA design flow	2 Hrs	➔ How to write constraint files in Vivado	3 Hrs
➢ Introduction To combinational Circuits and its various examples	2 Hrs	➔ Synthesis of combinational logic Examples	3 Hrs
➢ Introduction To Sequential Circuits and its various examples	2 Hrs	➔ Synthesis of sequential logic Examples	2 Hrs
➢ Introduction To FSM Circuits and its various examples	2 Hrs	➔ Synthesis of FSM Examples	2 Hrs
➢ Introduction To ASM Circuits and its various examples	2 Hrs	➔ How to use IP in Vivado	3 Hrs
➢ VHDL Function, Procedures & Declarations ➢ Verilog Function & Tasks	3 Hrs	➔ Practice Examples ➔ Examples Using Basys-3 Board	6 Hrs
➢ Mini Project (Real time project)	1 Hrs	➔ Complete Mini Project	1 Hrs