CPLD based power management system for low power devices

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Abstract

Energy is a precious resource in Wireless Sensor Nodes. With each transmission/reception and computation, energy is being consumed and batteries get drained. The problem gets critical when the network is implemented under harsh environmental conditions like forests. Thus energy harvesting from environment becomes an important concern especially in case of WSN due to power concerns. In this paper a design is presented for the development of power management system in wireless sensor nodes. The design presented utilizes solar energy to improve the efficiency and duration of operation for sensor nodes. Experimental setup shall comprise of a PV based array simulator and a CPLD based power management module.

KEYWORDS

CPLD, WSN, Super Capacitor, PV-Array, MPPT, VHDL, insolation, fan-in, pin to pin delay, deep discharge.

Introduction

Wireless Sensor Nodes are small low power intelligent devices which collect data from the environment: such as temperature, air pressure value, wind speed etc and transmit this data to other nodes and a central system creating a Wireless Sensor Network. Wireless sensor Nodes have gained tremendous popularity over the years due to their potential of being deployed under extreme harsh environments like forest fires and areas of natural disaster.

Currently low power sensing devices avail us with an opportunity to use small solar panels that can deliver enough power for both charging the batteries and supply the power to the sensing nodes [1].Thus main criteria for designing an efficient power management system should be to hold the stored energy and efficiently transfer power to load ends, besides taking care of getting sufficient energy from the solar panels [2]. Selection of components thus becomes essential for designing a system that can efficiently deliver power at relatively low current values.

This paper describes the design of a power management system for scavenging solar energy and efficiently transferring power to sensor nodes to improve their operational time. The system is composed of a PV array module and a power management module. The power management module is realized through Complex Programmable Logic Device (CPLD) due to its fast pin to pin performance and wide fan in of the macro cells, alternatively the PV-array is designed with a programmable PV module with capability to program different insolation/temperature profiles under laboratory conditions.

Background

Although currently low power sensing devices are available but these devices fundamentally rely on batteries for their operation. Batteries being extremely reliable sources of energy have limited operational time and need to be charged periodically. This limitation gets more exposed when the sensors are deployed under hostile environmental conditions and it becomes almost impossible to either recharge or exchange the discharged battery with a fresh one. This conventional power supply system is modified through the use of energy harvesting techniques which uses an energy conversion transducer tied to an intelligent power management system [5].

Many systems have been developed for powering sensor nodes using the architecture shown in Fig1 [3],[4]. Such systems are divided into two categories: Some are completely based on integrated circuits and do not use any logical controller [6] while others use microcontroller for performing power management related logical tasks[7]. Both of these systems utilize a large amount of harvested energy in driving the complex hardware setup on which they are designed. Moreover in microcontroller based systems pin to pin delay plays a vital role in control mechanism [?]. For this reason we aim to design a

control mechanism based on Complex programmable logic device (CPLD). A CPLD is chosen because of its fast pin to pin performance and wide fan in of macro cells [8].

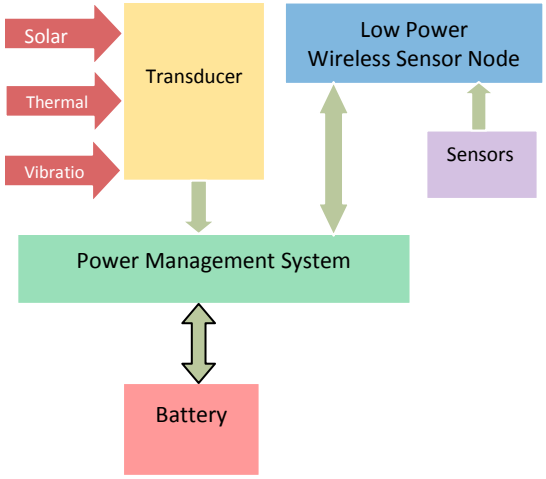

Figure 1: Energy Harvesting through Intelligent Power Management

System Design

Fig 2 depicts the block diagram of the proposed design, solid lines represent power flow, dashed arrow lines represent control flow through CPLD and the solid bold lines represent sample signals fed to CPLD through ADC. PV-Array is a solar panel capable of delivering power below 200mW range.
An additional footprint is included as a pilot cell for providing MPPT reference voltage.

Low Power Boost Converter

This module transfers energy from the PV Array to the super capacitor and battery. Boost converters like BQ25504RG from Texas Instruments can implement boost conversion with adjustable input voltage regulation [9]. Thus by means of a CPLD, we can supply a desired reference voltage to the device to achieve Maximum Power Point Tracking.

Power Storage Units

The system is implemented using a dual source architecture. Two energy storage units are used to supply power to the load. A super capacitor (S.C) of a very large capacity (5F) which supplies energy constantly even during no light conditions and a Li-ion battery which acts as a secondary buffer to S.C

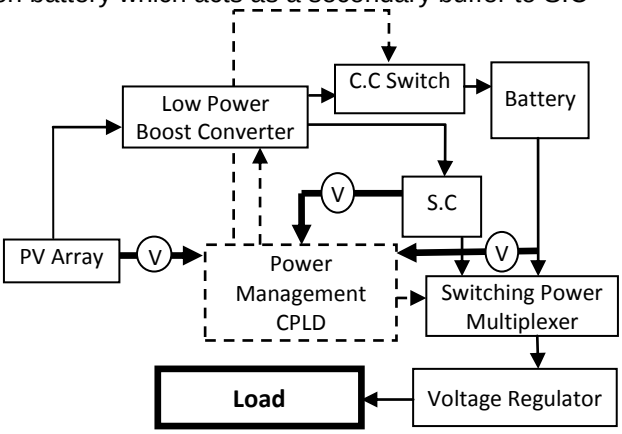

Figure 2: Block Diagram of Proposed System

Switching Multiplexer

An automatic power multiplexer selects the power path to the load. It switches automatically between S.C and the battery depending upon the voltage across S.C. Currently switching power multiplexers are available with very low current ratings between 0.5uA to 15uA.

Power Management (CPLD)

A complex programmable logic device having 256 macro cells and 100 pins is suggested for the design. VHDL is expected to achieve the following CPLD responsibilities:

- Monitor the S.C voltage, battery voltage and Current.
- Generate control signals for switching multiplexer and charge control switch.
- Determine which energy source can be used to power the Load.

To facilitate low power operation, the clock frequency of the CPLD should be selected to be as low as possible, as the power consumption is proportional to frequency [11].

Charge Monitoring

CPLD's charge monitoring capability is implemented by using voltage measurements of the battery. The voltage delivered by the battery gives an indication of how much capacity the battery has [10]; a typical Li-ion battery capacity is depicted in Fig 3.

Fig 3 indicates that if the battery voltage drops below 2.5V, the battery goes into deep discharge state

which should be avoided for better performance of the battery. In order to boost the battery life partial discharge cycles using only 20% or 30% of the battery capacity should be used. Fig 4 shows the logical flow diagram of the battery charging mechanism.

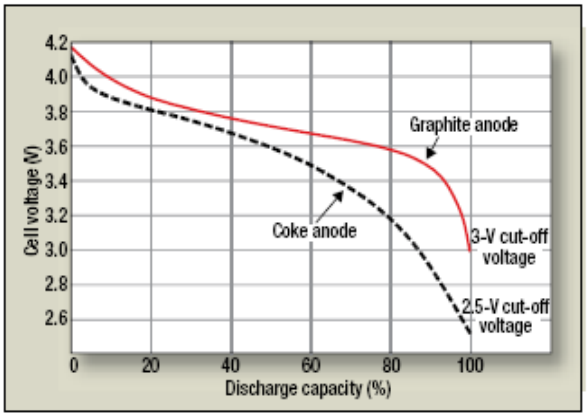

Figure 3: Voltage Vs Discharge capacity of Li-ion battery

With the data available to CPLD, a power management strategy can be implemented for long operation of sensor nodes.

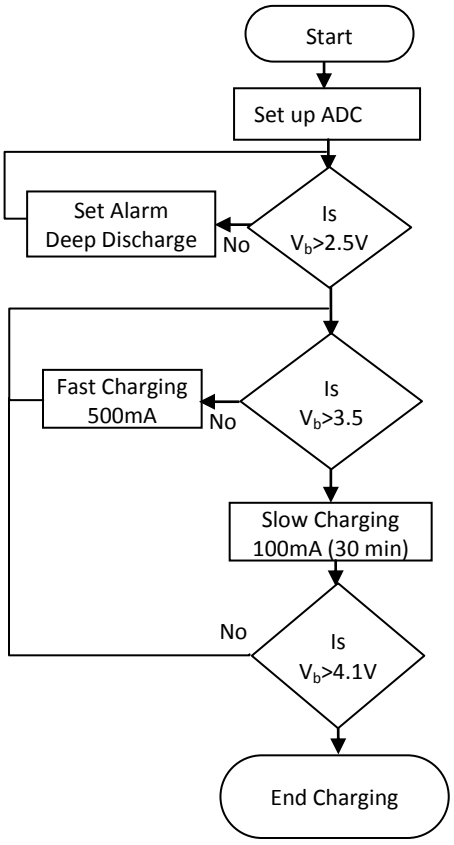

Figure 4: Charge Monitoring Flow Diagram

Main features of the proposed design

Reduced cost

Keeping in view the battery maintenance, over all cost of the system will be reduced since the battery life will improve and the batteries need not to be replaced frequently.

Flexibility

The design is perfectly suited to remote area applications. CPLD can be programmed for any desired task. If properly designed, the system controller can operate indefinitely with little supervision.

PV-Array Simulations

PV array simulator using PWM for duty cycle control is presented for the experimental setup. This kind of simulator will overcome the limitations of conventional setup like cost, time dependence and limited area of exposure [?].

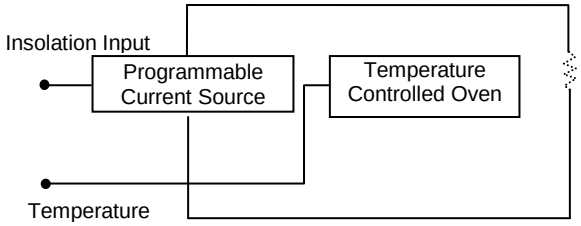

Figure-5: Generalized Block

The block diagram of PV – Array system is shown in Fig.5. The system is partitioned into programmable current source where varying short-circuit current indicates different insolation levels and a temperature controlled oven where variation in temperature would change the open-circuit voltage.

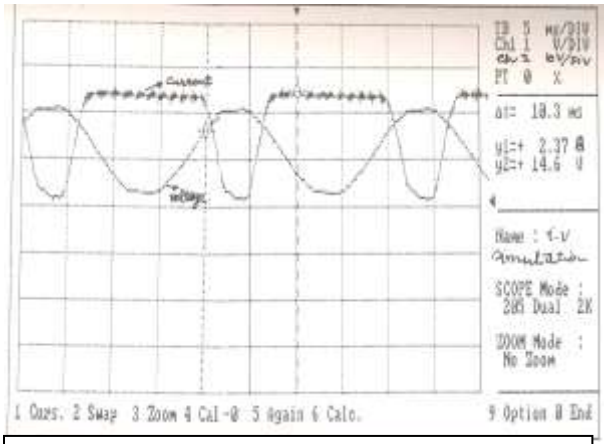

Figure-6: Current and Voltage Waveforms at the Output

(Isc=1Amp, Voc = 20 Volts

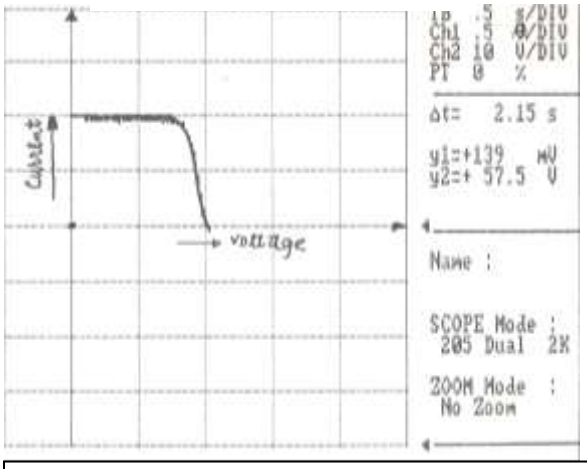

Figure-7 I-V Characteristics of PV Array Simulator

Test Results

Test results of PV – Array simulator are shown in Fig 6 and 7 respectively. The simulator has the potential to replace conventional simulator which is highly energy inefficient.The I-V characteristics generated are similar if not identical to that of a PV-module.

Conclusion

Hardware design of a power management scheme using dual energy storage system is presented. The proposed system is expected to reduce the energy usage and maintenance cost of low power devices like WSN. All the necessary power management functions are employed through low cost CPLD. An efficient charge monitoring mechanism is proposed which will improve the battery performance by preventing over charge and deep discharge conditions.

Future Work

Current design is totally dedicated to power management of sensor nodes but our actual aim is to automate the power control mechanism of complete sensor node structure including microcontroller, radio and sensors as well.

Several essential aspects remain yet to be under covered and are planned to be done in future. First a simulation based on present design need to be carried out to check the performance of the system and then the actual hardware implementation shall be carried out.

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