

Verilog Programming

Verilog Programming 2 Weeks Online Course

2 Weeks (2 Hrs. per day)

Timing: - 10:00 AM to 12:00 PM

Objective

The objective of the course is to take a lab oriented hands on practical approach for learning Verilog Programming via examples with more complete discussion. Numerous examples are provided to Learn and Re-Learn

B.E/B.Tech./MCA/BCA/M.Sc./B.Sc./BCA/
MCA/3Year Diploma in Electronics/ Electrical/
Instrumentation/ Computer Science / (pursuing also)

Eligibility

Prerequisite

- ✓ Candidate must have latest computer/laptop with preferably 4 GB RAM or higher and Graphics Card (2 GB)
- ✓ Software: Modelsim Altera (Freeware can be downloaded from <https://modelsim-altera-starter-edition.software.informer.com/13.1/>)
- ✓ Internet connection with good speed (*preferably 2 Mbps or higher*)

Rs. 1000/- incl. GST & all other charges.

Course Fees

Certificate

Certificate will be provided to the participants, based on minimum 75% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

- ✓ Instructor-led live classes.
- ✓ Instructor-led hands-on lab sessions.
- ✓ Content Access through e-Learning portal.
- ✓ Assessment and Certification

Methodology

How to Apply

- ✓ **Step-1:** Read the course structure & course requirements carefully.
- ✓ **Step-2:** Visit the Registration portal and click on apply button.
- ✓ **Step-3:** Create your login credentials and fill up all the details, see the preview and submit the form.
- ✓ **Step-4:** Login with your credentials to verify the mobile number, email ID and then upload the documents, Lock the profile and Pay the Fees online, using ATM-Debit Card / Credit Card / Internet Banking / UPI etc.

Course Content

| Day | Topic | Day | Topic |
|--------|------------------------------|--------|---|
| Day#01 | Introduction to Verilog | Day#06 | GENERATE Statement CONDITIONAL Statement |
| Day#02 | “Always” Block for Beginners | Day#07 | CASE Statement CASE GENRATE Statement |
| Day#03 | All Modeling Styles | Day#08 | TEST BENCH |
| Day#04 | Verilog Data Types | Day#09 | FSM in Verilog |
| Day#05 | Verilog Operators | Day#10 | Mealy and Moore State Machine Design |

Course Coordinator

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