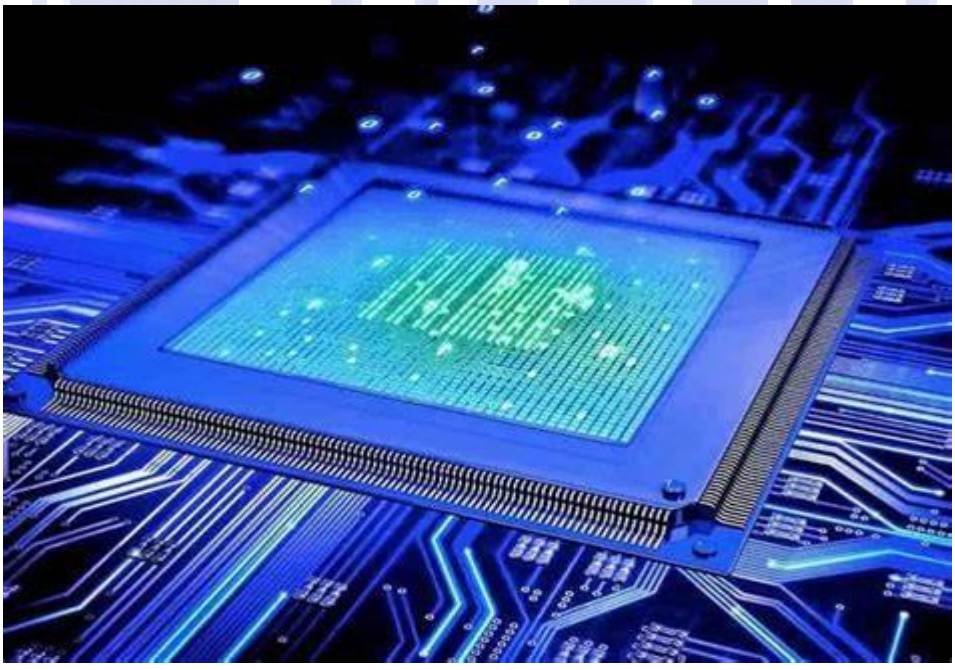
नेशनल इंस्टीट्यूट ऑफ इलेक्ट्रॉनिक्स एंड इंफॉर्मेशन टेक्नोलॉजी, चेन्नई
National Institute of Electronics and Information Technology, Chennai
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

Course Prospectus

Certificate course in

FPGA Prototyping using Verilog HDL

Mode: Online



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Course Prospectus

Course Name: Certificate course in FPGA Prototyping using Verilog HDL(Online Mode)

Course Code: ES 100

Duration: 90

Last Date of Registration: 26-02-2023

Date of publishing Provisional Selection List: 27-02-2023

Course Start Date: 1-03-2023

Fee Details:

Registration cum Course Fee- Rs. 1500/-

Preamble:

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general-purpose processors and ASICs. In particular, high-performance systems are now almost always implemented with FPGAs.

As per the recently published data, there are over 20,000 engineering professionals working in more than 150 companies in the chip designing industry and there is a huge demand for high-quality trained manpower in this field. This program will enhance the career opportunities of the participants in upskilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Objective of the Course:

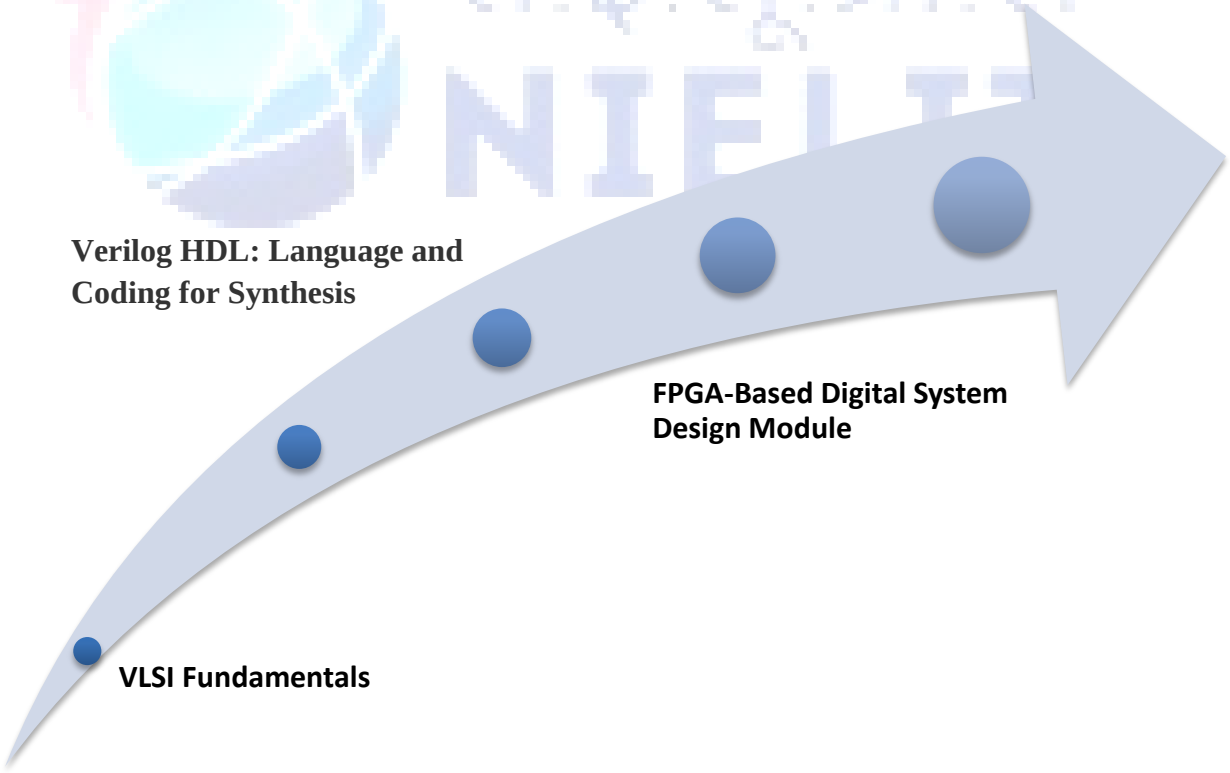
Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. In this process, participants will acquire expertise on entire logic design process and will be able to take on the challenges posed by chip design industry.

Outcome of the Course:

After successful completion of this Course, students will be able to:

- Understand brief history, present and future and Design Cycle of VLSI technology. Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax. Level of Abstraction in Verilog programing writing and simulating test benches in Verilog.
- Design and Develop IPs for VLSI using Verilog HDL and prototype them on FPGAs
- Emulate, debug & Characterize reusable IPs

Full Flow of Course



Course Structure

This course contains a total of 3 modules Candidate need to qualify for each module to qualify for the Certificate course in FPGA Prototyping using Verilog HDL.

Module Code	Module Name	Duration(in Hours)
ES 101	VLSI Fundamentals	5
ES 102	Verilog HDL: Language and Coding for Synthesis	15
ES 103	FPGA-Based Digital System Design Module	10
	Total Duration	**30**

Registration cum Course Fee.: Rs. 1500/-

(**Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible.)**

However, the above registration fee shall be refunded on few special cases as given below

- ✓ Candidates are eligible but not selected for admission.
- ✓ Course postponed and new date is not convenient for the student.
- ✓ Course cancelled.

Eligibility

Final Year Polytechnic Diploma in Electronics/Electrical/ Instrumentation

Or 3rd semester onwards B.E/B.Tech in Electronics/Electronics & Communication/ Electrical/ Electrical & Electronics/Instrumentation

Number of Seats: 35

Note: Seats are allocated based on the merit of the Qualification.

How to Apply?

Candidates can apply online in our website http://reg.nielitchennai.edu.in. Payment towards non-refundable registration fee can be paid through any of the following modes:

- ✓ Online transaction: Account Name: NIELIT CHENNAI, Account No: 31185720641, Bank name: State Bank of India (SBI), Branch: Kottur (Chennai), IFSC Code: SBIN0001669.
- ✓ Pay through UPI Mobile Apps

Note: *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

Last date of Registration: 26-02-2023

Registration Procedure

All interested candidates are required to fill the Registration form online with registration cum course fees before **26th February, 2023** with all the necessary information.

Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The Lit of Provisanally Selected Candidates will be published on NIELIT Chennai website (www.nielit.gov.in/chennai) **27th February, 2023** by **5:00 PM**.

- ✓ Following documents of candidates will be verified:
  - Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheet.
  - One passport size photograph.
  - Self-attested copy of Govt. issued photo ID card
  - AADHAR Copy

- ✓ Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

Admission:

All provisionally selected candidates whose documents are verified and paid the fees and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credential and URL for online portal will be shared through WhatsApp or email.

Discontinuing the course

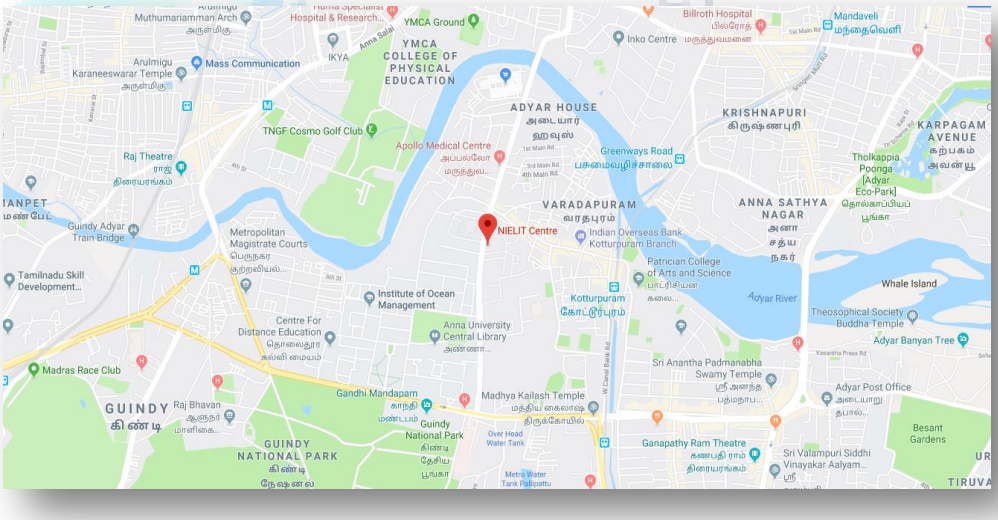
- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

Location:

NIELIT Chennai is located at Gandhi Mandapam Road, Kotturpuram, Chennai (Landmark: Opp.To Anna Centenary Library).



Address:

National institute of Electronics and Information Technology
ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025
E-mail: ishant[at]nielit[dot]gov[dot]in/ Phone: 044-24421445

Contact Person: Mr. Ishant Kumar Bajpai Mobile: 99580 16673 (Call @ 9 AM to 6 PM)

Course enquiries

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

Placement:

Students, who have completed the course successfully and qualified, will be given placement guidance and career counselling to crack the interviews.

Important Dates

Last Date of Registration: 26-02-2023

Date of publishing Provisional Selection List: 27-02-2023

Course Start Date: 1-03-2023

Examination & Certification

- ✓ Final Certificates will be issued after successful completion of all the modules. For getting certificate a candidate has to pass each module individually with minimum required marks of 50%.

Examination Scheme

Examination scheme for each module is as follows:

Module Name	Total Marks	Written	Practical / Assignment
VLSI Fundamentals	**50**	10	40
Verilog HDL: Language and Coding for Synthesis	**50**	10	40
FPGA-Based Digital System Design Module	**50**	10	40
Total	**150**	**30**	**120**

Grading Scheme

- ✓ Following Grading Scheme (on the basis of total marks) will be followed:

Grade	**S**	**A**	**B**	**C**	**D**	**Fail**
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

- ✓ Final Grading as per above grading scheme will be given on the basis of total marks obtained in all modules.

Lab Infrastructure Details:

Hardware Facilities:

- ✓ FPGA-Zed Board,
- ✓ Kintex, Virtex, Zynq,
- ✓ DE0 Development,
- ✓ Anvyl & Atlys Spartan-6,
- ✓ Zybo Board

Software Facilities:

- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ Matlab

Director, NIELIT Chennai

Dr. Pratap Kumar S

Director

Dr. Pratap Kumar S, is B.Tech (Electrical Engineering), M.Tech (Digital Electronics), MBA (Marketing) and PhD (Strategic Management). He has More than 29 years' experience in planning and execution of industrial consultancy projects, and capacity building projects funded by both industry and central & state ministries. Executed 7 major industrial consultancy projects and associated with the development of more than 50 product technologies, empowered more than 10,000 candidates through various capacity building programs and facilitated more than 40,000 job seekers through various job fairs and outreach programs. He has expertise in Strategy, Product Development, Automotive Electronics, Embedded Systems, and Power Electronics.

Faculty Profile:

Ishant Kumar Bajpai

Scientist 'C'

Ishant Kumar Bajpai, Scientist 'C', NIELIT Chennai Has more than 8 years' experience in Coordination and Implementation of funded projects in the area of IoT and VLSI with the application in Biomedical & Automotive. He has successfully executed 1 funded capacity building project in Karnataka & Kerala State and involved in the implementation of 4 skill development /capacity building projects funded by MeitY in the states of Tamil Nadu, Andhra Pradesh and Telangana. Before joining the NIELIT, he was working as a Scientific Officer in the IT Research Academy Division of Digital India Corporation (erst. Media Lab Asia), where he was involved in the Project Planning, Design and Implementation of projects in the domain of Mobile Computing, Networking & Applications.

ANUMOL C S

Resource Person- (Embedded & VLSI)

Anumol C S, Resource Person- Embedded and VLSI having knowledge in VLSI domain with the background of MTech in Electronics and Communication Engineering.

Annexure

Detailed Syllabus of the Course

Detailed Syllabus:

ES 101: VLSI Fundamentals

Module Duration: 10 Hours

Objective

The objective of the module is to provide a detailed review of VLSI fundamentals for a thorough understanding of the concepts and techniques for analog and digital system design.

Course Description

- CMOS Amplifiers & Applications
- Combinational Circuit Design
- Sequential Circuit Design including clocking and reset concepts
- Design of controller and Data path units
- State Machines
- Layout Design rules and Stick Diagrams

Learning Outcomes

On successful completion of the module, the candidate shall be able to:

- Design and analyze analog as well as digital systems

Reading List

1. Design of Analog CMOS ICs - Razavi. The best book available on CMOS analog.
2. Microelectronic circuits : Adel Sedra and Kenneth C. Smith
3. Franco S, Design with Operational Amplifiers and Analog Integrated Circutis
4. CMOS Analog circuit design - Allan and Holberg
5. Analog Integrated Circuit Design - Ken Martin and David Johns
6. Digital Design by Morris Mano & Michael D Ciletti
7. Digital Design: Principles and Practices by John F. Wakerly
8. Digital Design by Frank Vahid

ES 102: Verilog HDL: Language and Coding for Synthesis

Module Duration: 15 Hours

Objective

The objective of the course is to provide a thorough understanding of and hands-on with digital design & Verification using Verilog HDL

Course Description

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports, and Module Instantiation Methods
- Gate Level Modeling
- Dataflow Modeling
- Behavioral Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Mini-project and Case Studies

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Design IPs for VLSI using Verilog HDL
- Develop Test benches using Verilog HDL

Reading List

1. Verilog HDL - A guide to Digital Design and Synthesis by Samir Palnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi
5. Fundamentals Of Digital Logic With Verilog Design by Stephen Brown
6. Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL by Michael D. Ciletti
7. The Verilog Hardware Description Language by Donald E. Thomas & Philip R. Moorby
8. IEEE Std 1364-2005 : IEEE Standard Hardware Description Language based on the Verilog Hardware Description Language by the IEEE

ES 103: FPGA Based Digital System

Design Module Duration: 10 Hours

Objective

The objective of the course is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation

Course Description

- Introduction to Programmable Logic and FPGAs
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow Xilinx Vivado®
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Implementation Details and optimization techniques
- Static Timing Analysis
- Introduction to AXI4/Avalon Interfaces
- Design problems using Xilinx® Platforms

- Case Studies on FPGA-Based implementations

Learning Outcomes

After successful completion of this module, students should be able to:

- Prototype digital Systems using FPGA
- Emulate, debug & Characterize reusable IPs

Reading List

1. FPGA-Based System Design by Wayne Wolf
2. Advanced FPGA Design Architecture, Implementation and optimization by Kilts
3. Xilinx® User guides & documentation available at https://www.xilinx.com/support /documentation-navigation/overview.html
4. Intel® FPGA User guides & documentation available at https://www.intel.com/ content/www/us/en/programmable/documentation/lit- index.html
5. Swadeshi Microprocessors user guides & documentation available at available at https://shakti.org.in/
6. Embedded Core Design with FPGAs. by Zainalabedin Navabi
7. FPGA Prototyping by Verilog Examples by Pong P. Chu
8. Digital Design Using Digilent FPGA Boards Verilog / Vivado Edition Richard E Haskell, Darrin M Hanna
9. FPGA Design: Best Practices for Team-Based Reuse by Philip Andrew Simpson

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