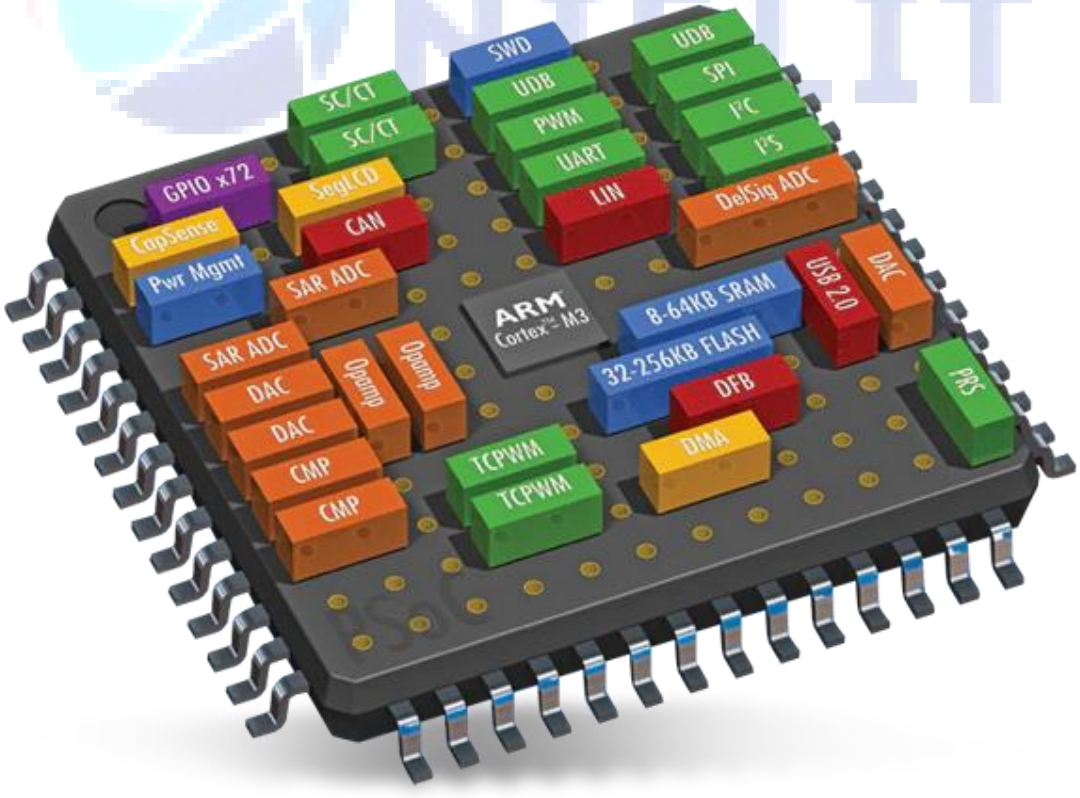
राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, चेन्नई
National Institute of Electronics & Information Technology, Chennai
Ministry of Electronics & Information Technology
Government of India

नेशनल इंस्टीट्यूट ऑफ इलेक्ट्रॉनिक्स एंड इंफॉर्मेशन टेक्नोलॉजी, चेन्नई
**National Institute of Electronics and Information Technology, Chennai**
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

# Course Prospectus

# PG Program in Embedded and SoC Design

## **Mode:** Online



# Index

# Course Prospectus

**Course Name:** PG Program in Embedded and SoC Design (Online Mode)

**Course Code:** ES 600

**Duration:** 840 Hours, 6 Months

**Last Date of Registration:** 24-09-2023

**Date of publishing Provisional Selection List:** 25-09-2023

**Payment of first instalment fee:** 25-09-2023 to 26-09-2023

**Course Start Date:** 27-09-2023

**Fee Details:**

Registration Fee- Rs. 1,000 /- (Adjusted with Total Fee)

Total Fee - Rs. 52,000 /-

## Preamble:

The emergence of India as a global economy has opened up a huge demand for electronic products. National Policy on Electronics and Make in India initiative of the Government of India has resulted in the setting up of many industries in the Electronics sector and has led to a huge demand for trained manpower in the Embedded and VLSI. With the development of semiconductor process technology, more and more transistors are integrated into a single chip. As consequence, Integrated Circuits (ICs) can now host more functionality on one chip, leading us to the System-on-Chip (SoC) era.

Today SoC is prevalent in all kinds of electronics systems. From embedded systems to cloud computers, SoCs are being used in various configurations for versatile types of tasks. The growing class of complex applications such as machine learning and image processing makes it difficult for engineers to close the increasingly severe productivity gap that arises from the integration of hardware and software. The complexity challenge can only be tackled by well-trained engineers with good understanding of the requirements and challenges at all levels of the design process. Hence, there need an advanced training program that promote the integration of hardware and software as a single discipline. This course focuses on the architecture and programming of embedded processors and its implementation on the target FPGA platform.

## Objective of the Course:

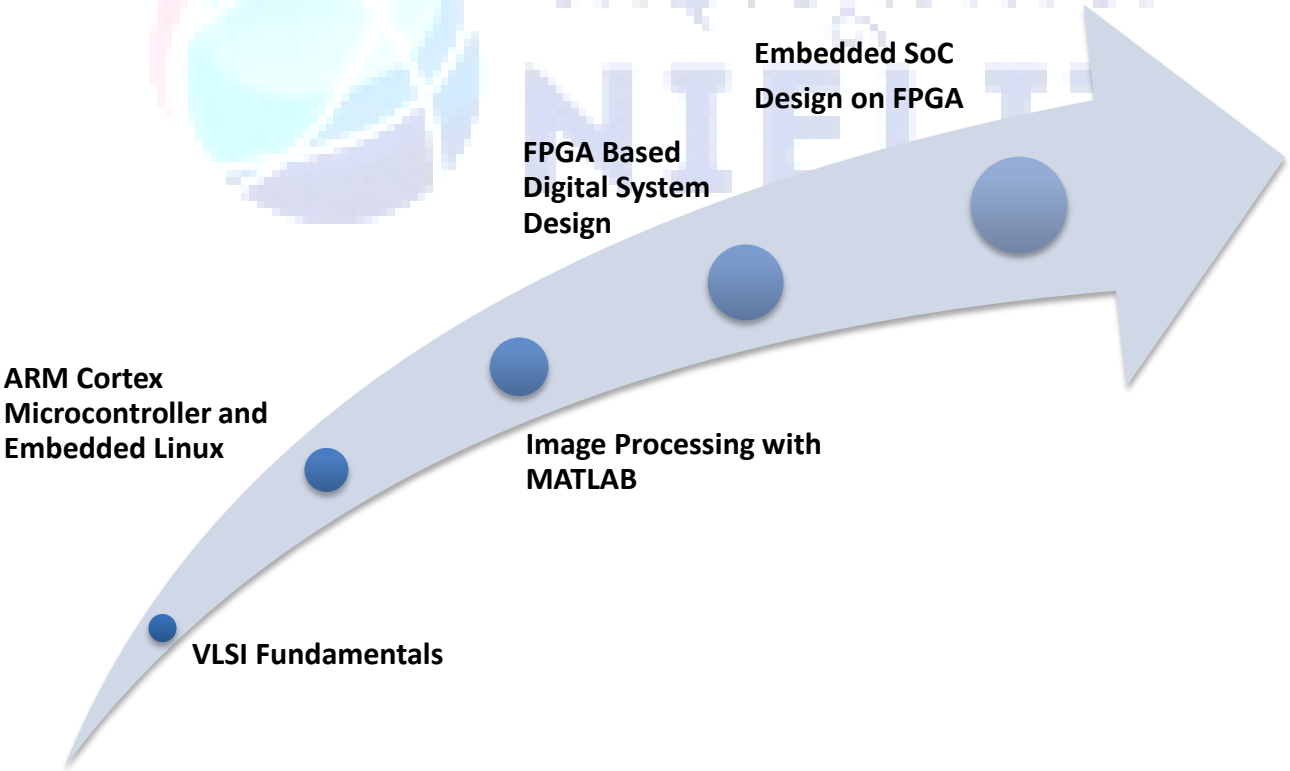
To develop the skill set required for the Design and Development the Embedded System Applications using suitable Hardware and Software tools and its implementation on the target FPGA platform. The qualifiers will acquire hands-on experience in embedded system design, state-of-the-art design methodologies and platforms. The program is an immediate relevance to industry and makes the participants exactly suitable for Embedded and VLSI Industry

## Outcome of the Course:

After successful completion of this Course, students will be able to:

- Develop Embedded Application using ARM Cortex Microcontroller with Embedded- C Programming.
- Implement the Image Processing algorithms using MATLAB
- Design and Develop IPs for VLSI using Verilog HDL and prototype them on FPGAs
- Create their own IP and SoC design for FPGA implementation
- Develop their own software application with Zynq APSoC

## Full Flow of Course



## Course Structure

This course contains totally Nine modules. After completing the first Eight modules, the students have to do a six weeks project using any of the topics studied to earn the PG Program in Embedded and SoC Design certificate.

| Code | NOS Name | Duration(in Hours) |
|---|---|---|
| **ES 601** | VLSI design methodologies and principles | 60 |
| **ES 602** | Embedded System Design with Embedded C Programming on ARM Cortex Microcontrollers | 150 |
| **ES 603** | Implementation of Complex Embedded Systems using Suitable Operating Systems | 60 |
| **ES 604** | Implementation of Image/Signal Processing algorithms Using MATLAB/Python | 90 |
| **ES 605** | Verilog hardware description languages (HDLs) to design RTL circuits | 60 |
| **ES 606** | Prototype digital circuits on FPGA using HDLs, analyze and debug | 60 |
| **ES 607** | Embedded SoC Design on FPGA | 60 |
| **ES 609** | Employability Skills | 90 |
| **ES 610** | Project Work/OJT | 210 |
| **Total Duration** | | **840** |

## Course Fees

The course fee is Rs. 52,000/- Including GST. (Can be paid as a single installment of Rs. 52,000/- or in 2installmentss as given below)

| Registration Fee | Rs. 1000/- for SC-ST (Adjustable with total fee) | Rs. 1000/- for others (Adjustable with total fee) | |
|---|---|---|---|
| Instalment No. | SC-ST Candidates (Fee including GST in Rs.) | General Candidates (Fee including GST in Rs.) | Last Date |
| 1 | 3,500 | 25,500.00 | 26-09-2023 |
| 2 | Nil | 25,500.00 | 26-12-2023 |
| Total | 4500 | 52,000.00 | |

**GST is Applicable as per Govt. Norms GST (currently it is 18%).*

## Registration Fee.

(**Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible.)**

SC/ST: Rs. 1,000/- (Adjustable with Total fee for candidates).

Others: Rs. 1,000/- (Adjustable with Total fee for candidates)

However, the above registration fee shall be refunded on few special cases as given below

- ✓ Candidates are eligible but not selected for admission.
- ✓ Course postponed and new date is not convenient for the student.
- ✓ Course cancelled.

## Eligibility

- ✓ B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Biomedical /Computer Science/Information Technology
  or
- ✓ M.Sc. (Electronic) in Electronics/ Electronics & Communication.
  or
- ✓ 2-year Diploma after 12th with 2 year experience in VLSI/Embedded Domain

## Number of Seats: 30 – Total

| Category | No. of Seats |
|---|---|
| **SC (15%)** | 4 |
| **ST (7.5%)** | 2 |
| **GENERAL** | 24 |
| **Total** | **30** |

**Note**: Seats are allocated based on the merit of the Qualification.

## How to Apply?

Candidates can apply online in our website http://reg.nielitchennai.edu.in. Payment towards non-refundable registration fee can be paid through any of the following modes:

- ✓ Online transaction: Account Name: NIELIT CHENNAI, Account No: 31185720641, Bank name: State Bank of India (SBI), Branch: Kottur (Chennai), IFSC Code: SBIN0001669.

- ✓ Pay through UPI Mobile Apps

**Note**: *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

## Last date of Registration: 24-09-2023

## Registration Procedure

All interested candidates are required to fill the Registration form online with registration fees before **26-09-2023** with all the necessary information.

## Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The first list of Provisionally Selected Candidates will be published on NIELIT Chennai website (www.nielit.gov.in/chennai ) **25-09-2023** by **5:00 PM**. In case of vacancy, an additional selection list will be prepared and the selection will be intimated by email only.
- ✓ Provisionally selected candidate has to upload their document on registration portal for online verification.
    - Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheet.
    - One passport size photograph.
    - Self-attested copy of Govt. issued photo ID card
- ✓ After document verification, selected candidates have to pay first instalment of **Rs. 17,000/-** or as applicable on or before **26-09-2023** by payment mode mentioned above. Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

## Admission:

All provisionally selected candidates whose documents are verified and paid the fees (full or first instalment) and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credential and URL for online portal will be shared through WhatsApp or email.

## Discontinuing the course

- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

## Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

## Address:

**National institute of Electronics and Information Technology**
**ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025**
**E-mail: ishant[at]nielit[dot]gov[dot]in/ Phone: 044-24421445**

**Contact Person: Mr. Ishant Kumar Bajpai Mobile: 99580 16673 (Call @ 9 AM to 6 PM)**

## Course enquiries

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

## Placement:

Students who have completed the course successfully and qualified, will be given placement guidance and career counselling to crack the interviews.

## Important Dates

**Last Date of Registration:** 24-09-2023

**Date of publishing Provisional Selection List:** 25-09-2023

**Payment of first instalment fee:** 25-09-2023 to 26-09-2023

**Course Start Date:** 27-09-2023

**Payment of second instalment fee**: 26-12-2023

## Examination & Certification

- ✓ Final Certificates will be issued after successful completion of all the modules including mini project. For getting certificate a candidate has to pass each module individually with minimum required marks of 50%.

## Examination Scheme

Examination scheme for each module is as follows:

| Module Name | Total Marks | Written | Practical / Assignment |
|---|---|---|---|
| **VLSI design methodologies and principles** | **100** | 25 | 75 |
| **Embedded System Design with Embedded C Programming on ARM Cortex Microcontrollers** | **100** | 25 | 75 |
| **Implementation of Complex Embedded Systems using Suitable Operating Systems** | **100** | 20 | 80 |
| **Implementation of Image/Signal Processing algorithms Using MATLAB/Python** | **100** | 25 | 75 |
| **Verilog hardware description languages (HDLs) to design RTL circuits** | **100** | 20 | 80 |
| **Prototype digital circuits on FPGA using HDLs, analyze and debug** | **100** | 25 | 75 |
| **Embedded SoC Design on FPGA** | **100** | 25 | 75 |
| **Employability Skills** | **100** | 25 | 80 |
| **Project Work/OJT** | **100** | NA | 100 |
| **Total** | **900** | **190** | **710** |

## Grading Scheme

- ✓ Following Grading Scheme (on the basis of total marks) will be followed:

| **Grade** | **S** | **A** | **B** | **C** | **D** | **Fail** |
|---|---|---|---|---|---|---|
| **Marks Range (in %)** | 85 to 100 | 75 to 84 | 65 to 74 | 55 to 64 | 50 to 54 | Below 50 |

- ✓ Final Grading as per above grading scheme will be given on the basis of total marks obtained in all modules. For last module (ES 609) grade will be given on the basis of project demonstration.

## Lab Infrastructure Details:

**Hardware Facilities:**

- ✓ Development Boards - STM32, ARM Cortex-M4
- ✓ Sensors–PIR, Ultrasonic, Soil Moisture, Accelerometer & Gyro meter
- ✓ FPGA- Xilinx Kintex-KC705 Evaluation Kit, Xilinx Virtex - VC 707 Evaluation Kit, ZedBoard-Zyng-7000 Development Board
- ✓ DSP Evaluation Board – TI-EVK2H with Arm Cortex-A15 processor

**Software Facilities:**

- ✓ OpenSTM, CubeMX
- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ Matlab

## Student Testimonials

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### JOB PLACEMENT

**NAVEEK KUMAR THARASI**

Course Completed: June 2023

Senior Software Engineer, Wipro

Message

"I had the opportunity to attend PGP embedded & VLSI course at NIELIT Chennai, and I must say it was an exceptional learning experience. The course provided a comprehensive and in-depth understanding of embedded systems and VLSI design, equipping me with valuable knowledge and skills.

One of the aspects that made this course truly outstanding was the expertise and dedication of the faculty members. They were not just knowledgeable instructors but also excellent mentors. They provided guidance and support, addressing our queries and ensuring that we were able to apply the concepts practically. Their commitment to our learning journey was evident in their personalized attention and willingness to assist beyond the classroom.

I highly recommend the embedded & VLSI course at NIELIT Chennai to anyone looking to delve into these fascinating domains.

# JOB PLACEMENT

## Dr. Sachin Bahade

**Course Completed: June 2023**

Assistant Professor and Head Department of Electronics,
Nabira Mahavidyalaya, Katol, Dist. Nagpur

## Message

Overall the training was very excellent and I am very much thankful to NIELIT Chennai, faculties for their invaluable support and guidance throughout the coursework. It was a wonderful experience throughout the course. It was a very much interactive session by giving real-time experiences to understand it in a more practical manner. Their mentorship helped me to enhance my overall academic and professional development. I am fortunate to have had someone as acknowledgeable and supportive as them by my side during this process. The knowledge, skills, and practical experience I gained during the coursework were instrumental in preparing me for the challenges of the academic and professional world. The PG in embedded and SoC course provides thorough knowledge of embedded systems, Python, Matlab, Verilog, and VLSI design. Their dedication and commitment made a significant difference in helping me secure a position that aligned with my career goals.

## Faculty Profile:

### Shoukath Cherukat

Scientist 'E'

**Shoukath Cherukat**, Scientist 'E', NIELIT Chennai has more than 21 years of Experience in Teaching and Consultancy Projects. He has successfully completed Consultancy Activities such as Collimator Test JIG for OEN, Technology Development of Wireless Token Display System for Keltron, Integrated Microcontroller Development Systems for 8051 & 80C196 Microcontrollers (IMDS-51, IMDS-196 & IMDS-196D) supplied to various industries. He is having wide hands-on

experience in Embedded Controllers (8, 16 & 32-bit), Digital Signal Processors, FPGAs, IoT, Embedded OS and Real Time Operating Systems (RTOS).

**Ishant Kumar Bajpai**

Scientist 'D'

**Ishant Kumar Bajpai**, extensive experience spans over a decade and revolves around implementing funded projects in two key areas: the Internet of Things (IoT) and Very Large Scale Integration (VLSI) with applications in the Biomedical and Automotive industries. His research interests are focused on FPGA implementations of Digital Signal Processing (DSP) systems.

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**Chandralakha R Pillai**

Resource Person- (Embedded & VLSI)

**Chandralakha R Pillai,** Resource Person- Embedded and VLSI having 3 years of experience in edtech industry as well as hands on experience on PCB design in altium designer with the background of MTech in VLSI and embedded systems.

**S. Raghavendran**

Resource Person-RPA

**Raghavendran. S**, Resource Person RPA having 3 years of experience in Robotics and automation and handing training session and Labs on UiPath studio with the background of electronics and instrumentation.

# Detailed Syllabus of the Course

## ES 601: VLSI design methodologies and principles

## Module Duration: 60 Hours

**Objective:** The objective of the module is to provide a detailed review of VLSI fundamentals for a thorough understanding of the concepts and techniques for analog and digital system design.

## Module Description

**Introduction to VLSI Design**

- Overview of VLSI technology and its significance
- Introduction to VLSI design flow: Front-end and Back-end

**CMOS Transistor Theory**

- Fundamentals of MOSFET operation
- MOSFET characteristics and modeling
- MOSFET scaling trends and technology advancements

**CMOS Inverter Characteristics**

- CMOS inverter operation and voltage transfer characteristics
- Noise margin analysis and power consumption considerations
- Inverter sizing and optimization techniques

**CMOS Logic Design**

- Introduction to basic logic gates: AND, OR, NAND, NOR
- Combinational logic design using CMOS technology
- Designing complex logic functions using CMOS logic gates

**Transistor Level Schematics and Layouts**

- Transistor level design techniques
- Schematic design and layout considerations
- Design rules, metal layers, and interconnect routing

**On-Chip Wire Modeling**

- Introduction to on-chip interconnects
- Wire parasitics and their impact on circuit performance
- Modeling and simulation of on-chip wires

**Bonding Diagram, Packaging, and Assembly**

- Overview of packaging technologies and assembly processes
- Bonding diagram design and considerations
- Packaging trends and challenges

**Gate Delays and Logical Effort**

- Gate delay modeling and estimation
- Introduction to logical effort analysis
- Determining the best delay-power trade-off for logic gates using P/N ratio

**Combinational Logic Circuit Critical Path Optimization**

- Identifying critical paths in combinational circuits
- Gate sizing and logic restructuring techniques
- Timing optimization for improved performance

**Timing in Sequential Circuits**

- Introduction to sequential circuits: flip-flops, registers
- Setup and hold time analysis
- Sequential circuit timing considerations and optimization techniques

## Learning Outcomes

The Qualifier of the NOS should be able to:

- Construct digital logic gates using CMOS technology
- Analyze and optimize the performance of digital gates
- Anticipate the impact of parasitics and technology scaling
- Implement a semi-custom integrated circuit from a given RTL code to layout
- Link simplified abstract models to detailed computer simulations

## Reading List

1. Design of Analog CMOS ICs - Razavi. The best book available on CMOSanalog.
2. Microelectronic circuits : Adel Sedra and Kenneth C. Smith
3. Franco S, Design with Operational Amplifiers and Analog Integrated Circutis
4. CMOS Analog circuit design - Allan and Holberg
5. Analog Integrated Circuit Design - Ken Martin and David Johns
6. Digital Design by Morris Mano & Michael D Ciletti
7. Digital Design: Principles and Practices by John F. Wakerly
8. Digital Design by Frank Vahid

## ES 602: Embedded System Design with Embedded C Programming on ARM Cortex Microcontrollers

### Module Duration: 150 Hours

**Objective:** To set the required background in embedded system concepts, Embedded 'C' language such as Memory Management, Pointers, Data structures, and architecture of the ARMCortex processor for highly deterministic real-time applications.

### Module Description

**'C' and Embedded C:**
Introduction to 'C' programming, Storage Classes, Data Types, Control Structures, Arrays, Functions, Memory Management, Pointers, Arrays and Pointers, Pointer to Functions and advanced topics on Pointers, Structures and Unions, Data Structures, Linked List, Stacks, Queues, Pre-processor directives, File operations, Variable arguments in Functions, Command line arguments, bitwise operations, Typecasting.

**Embedded Concepts:**
Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of Embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools**.**

**Introduction to ARM Cortex Architecture:**
Introduction to 32-bit Processors, The ARM Architecture, Overview of ARM, Overview of Cortex Architecture, Cortex M4 Register Set and Modes, Cortex M4 Processor Core, Data Path and Instruction Decoding, ARM Cortex M4 Development Environment, Assembler and Compiler, Linkers and Debuggers, ARM, Thumb & Thumb2 instructions, Mixing ARM & Thumb Instructions, Memory hierarchy, Memory Mapping, Cache.

**Cortex M4 Microcontrollers & Peripherals:**
Cortex M4-based controller architecture, Memory mapping, Cortex M4 Peripherals – RCC, GPIO, Timer, System timer, UARTs, LCD, ADC, Cortex M4 interrupt handling –NVIC. Application development with Cortex M4 controllers using standard peripheral libraries.

### Learning Outcomes

After successful completion of the module, the students will be able to:

- Participants will be able to develop Embedded applications using Embedded C Programming
- Participant will be able to use ARM Cortex-Mx based Microcontrollers with EmbeddedC Programming for Application Development

### Text Books:

1. Embedded/Real-Time Systems Concepts, Design and Programming BlackBook,Prasad, KVK.
2. Let us C by Yashwant Kanetkar.
3. The Definitive Guide to the ARM Cortex M3, Joseph Yiu, Newnes.

### Reference Books:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, TataMcGraw Hill.
2. Embedded C, Pont, Michael J
3. Embedded Systems an Integrated Approach: Lyla B Das, Pearson
4. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
5. Art of C Programming, JONES, ROBIN,STEWART, IAN
6. ARM System Developer's Guide - Designing and Optimizing System Softwareby: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elseiver.
7. Cortex M3/M4 Reference manual.
8. STM32Ldiscovery datasheets, reference manuals & Application notes.

## ES 603: Implementation of Complex Embedded Systems using suitable Operating Systems

**Module Duration: 60 Hours**

**Objective:** To Skill the students in Configure, Deploying, and Debugging the Linux OS onto aTarget Board to build a complete Embedded Product using Linux Kernel.

### Module Description

**Introduction:**

Basic Operating System Concepts, History& Benefits of Linux, Fundamentals of Embedded Linux OS, Comparison of Embedded OS, Embedded OS Tools and IDE, Embedded Linux, Applications andProducts.

**Architecture of Embedded Linux:**

Types of kernels, Kernel Architecture Overview: User Space, Kernel Space, Kernel Functional Overview: File System, Process Management, Address Spaces and Privilege Levels, Memory Management, System Call, Inter Process Communication (IPC) – Pipes, FIFO & Shared Memory, Device Drivers, Network.

**Commands in Linux:**

Log in Linux system and Log in Remote Linux Systems-Getting Help Accessing & Working with the Command Line and Shell System Access, Entering Commands.

**Boot Methods:**
Creating User Accounts &Managing Users Creating Groups & Managing Groups, Directory Management, File Permissions and Ownership, Text Editor.

**Configuring the Linux Environment:**
Linux environment, Types of Hosts, Types of Host/Target Development Setups, Types of Host/Target Debug Setups, Embedded Environment Tools, GNU Tool-chain Cross Compilers.

**Tool-chain: Configuration and Cross-Compilation:**
Tool-chain. Native vs. cross-compilation, Toolchain Components, Toolchain choices, Using buildroot to build the toolchain, Configuration options, Adding path variables to start up scripts (.bashrc), CROSS_COMPILE variable, Validating the cross-compiler.

**Linux Bootloader & U-Boot:**
Boot-loader Phases, U-boot – Embedded boot loader, Navigating the u-boot sources, Configuring and Cross-compiling u-boot, installing u-boot on the target, understanding u-boot commands, changing environment variables to setup kernel booting, transferring files to the target using tftp.

**Embedded Linux Kernel:**
Kernel Features, Kernel Subsystems, Memory Manager, Scheduler, Embedded Storage, I/O Subsystem, Network Subsystem, Navigating the kernel sources, Kernel Configuration, Kernel Compilation Booting the kernel using u-boot, Module compilation and Installation to RootFS, Procedure for adding a new driver to the kernel, Applying patches.

**Building Root File System:**
Introduction to File system, Linux directory structure, Organization and Important directories,/dev file system, Steps after kernel booting, init and start-up scripts, Downloading & Compiling RootFS, RootFS in Flash/SD Card Storage.

**Porting OS in ARM Board:**
Kernel Compilation, Booting the kernel using u-boot, Porting Linux in ARM Board.

**Embedded Linux Application Programming:**
Application Developments using Input Devices, Application Developments using Output Devices, Application Developments using Peripherals.

## Learning Outcomes:

After successful completion of this module, Students will be able to:

- Set up a Linux environment for ARM-based Target Boards.
- Configure Tool-Chain for ARM Platforms.
- Understand Linux Booting Process and be able to configure Linux Kernels on ARM-based Embedded Boards.

- Develop ARM-based Embedded Applications with Linux OS.

**Reading List:**

1. GNU/LINUX Application Programming, Jones, M Tims
2. Embedded Linux: Hardware, Software, and Interfacing, Hollabaugh, Craig,
3. Building Embedded Linux Systems: Yaghmour, Karim
4. Embedded Software Primer: Simon, David E.
5. Linux Kernel Internals: Beck, Michael At Al
6. UNIX Network Programming: Steven, Richard
7. Linux: The Complete Reference: Petersen, Richard
8. Linux Device Drivers: Rubini, Alessandro, Corbet, Jonathan
9. Linux Kernel Programming: Algorithms and Structures of version 2.4:Beck,Michael At Al
10. Linux Kernel Development: Love, Robert
11. Operating System Concepts, Peter B. Galvin, Abraham Silberschatz,GergGagne, Wiley Publishers

## ES 604: Implementation of Image/Signal Processing algorithms Using MATLAB/Python

**Module Duration: 90 Hours**

**Objective:** The objective of the module is to provide a thorough understanding of and hands-onwith geometric Transformation of Imaging using MATLAB

**Module Description**

**Image Processing:**

Introduction to Image Processing, Notion of pixel, resolution, quantization, photon noise, Geometric transformations, source-to-target and target-to-source mapping, planar and rotational homography, Image registration and change detection, Motion Blur and Image Formation. Image Transform, Image Enhancement, Restoration, and Edge Detection Design Verification using Test benches. Typical image processing application implementation using MATLAB/Python

**Signal Processing:**

Introduction to DSP architectures and programming, Sampling Theory, Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), and Quantization; Decimation, Interpolation, Convolution, Simple Moving Average; Periodic Signals and harmonics; Fourier Transform (DFT/FFT), Spectral Analysis, and time/spectrum representations; FIR and IIR filters.

**Learning Outcomes:**

After successful completion of the module, the students shall be able to:

- Understand the geometric Transformation of the Image
- implement the Image Processing application using MATLAB/Python

- learn the basic theory of digital signal processing
- Implement fundamental DSP algorithms

**Reading List:**

1. Digital Image Processing by Gonzalez and Woods.
2. The essential guide to image processing by Alan Bovik.
3. Digital Signal Processing using MATLAB for Students and Researchers by John W. Leis
4. Introduction to Medical Imaging by Nadine Barrie Smith and Andrew Webb
5. Medical Imaging Signal and Systems by Jerry L. Prince and Jonathan M. Links

## ES 605: Verilog hardware description languages (HDLs) to design RTL circuits

### Module Duration: 60 Hours

**Objective:**The objective of the course is to provide a thorough understanding of and hands-onwith digital design & Verification using Verilog HDL

### Module Description

**RTL Design Methodology:**

- Basics of Register Transfer Level (RTL) design
- Overview of RTL design process and methodology
- Introduction to Hardware Description Languages (HDLs) - Verilog

**RTL Design Using HDL:**

- Introduction to Verilog syntax and construct
- Designing combinational and sequential logic using HDL
- Writing RTL code for basic digital circuits

**RTL Simulation and Verification:**

- Functional verification techniques for RTL designs
- Introduction to test benches and test bench development
- Simulation and debugging of RTL designs

**Timing Constraints and Analysis:**

- Introduction to timing constraints in RTL design
- Timing analysis and optimization techniques
- Setup and hold time violations and resolution

### Learning Outcomes:

After successful completion of the module, the students shall be able to:

- Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax, Level of Abstraction in Verilog programing andtest bench simulation.

- Design and Develop IPs for VLSI using Verilog
- Emulate, debug & Characterize reusable IPs

**Reading List:**

1. Verilog HDL - A guide to Digital Design and Synthesis by SamirPalnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi
5. Fundamentals Of Digital Logic With Verilog Design by Stephen Brown
6. Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDLby Michael D. Ciletti
7. The Verilog Hardware Description Language by Donald E. Thomas &Philip R. Moorby
8. IEEE Std 1364-2005 : IEEE Standard Hardware Description Languagebased on the Verilog Hardware Description Language by the IEEE

## ES 606: Prototype digital circuits on FPGA using HDLs, analyze and debug Design

**ModuleDuration: 60 Hours**

**Objective:** The objective of the course is to provide a thorough understanding about and hands-onpractice with FPGA based digital system design and emulation

**Module Description**

**Introduction to FPGAs:**

- Overview of Field-Programmable Gate Arrays (FPGAs) and their applications
- Advantages of using FPGAs in digital design

**FPGA Architecture and Components:**

- Understanding the internal architecture of FPGAs
- Basic components of an FPGA: Look-Up Tables (LUTs), flip-flops, interconnects, etc.
- Introduction to FPGA families and resources

**FPGA Design Flow:**

- Overview of the FPGA design flow and methodology
- Design entry, synthesis, placement, routing, and bitstream generation
- Introduction to design constraints

**FPGA Design Optimization Techniques:**

- Timing constraints and analysis in FPGA designs
- Pipelining, retiming, and other optimization techniques
- Trade-offs between area, power, and performance

### Learning Outcomes:

After successful completion of this module, students should be able to:

- Construct digital logic circuits using Verilog HDL
- Simulate those designs using industry-standard simulation tools
- Synthesis and port the design onto FPGA using industry-standard tools
- Implement a project of good complexity onto FPGA
- Debug the FPGA Designs with advanced FPGA tools.

### Reading List

1. FPGA-Based System Design by Wayne Wolf
2. Advanced FPGA Design Architecture, Implementation and optimization byKilts
3. Xilinx® User guides & documentation available at https://www.xilinx.com/support /documentation-navigation/overview.html
4. Intel® FPGA User guides & documentation available at https://www.intel.com/ content/www/us/en/programmable/documentation/lit-index.html
5. Swadeshi Microprocessors user guides & documentation available at availableathttps://shakti.org.in/
6. Embedded Core Design with FPGAs. by Zainalabedin Navabi
7. FPGA Prototyping by Verilog Examples by Pong P. Chu
8. Digital Design Using Digilent FPGA Boards Verilog / Vivado Edition RichardE Haskell,Darrin M Hanna
9. FPGA Design: Best Practices for Team-Based Reuse by Philip AndrewSimpson

## ES 607: Embedded SoC Design on FPGA

### Module Duration: 60 Hours

**Objective**: FPGA chips are especially useful for machine learning and Image processing. The objective of this module is to enable the qualifier to optimize throughput and adapt processors tomeet the specific needs of different Image processing/ML architectures.

### Module Description

**VLSI implementation architectures for Image Processing/ML:**

- Multi-core, many-core, and hardware accelerators
- Hardware acceleration of Image Processing Algorithms
- Design steps- Software Design Flow, Platform Project Creation, Application Project Creation, and Debugging using Xilinx Vitis
- Case Studies: Realization of Image Processing algorithms on FPGA

**Metrics for Analysis and Comparison of Architectures**

- Hardware performance matrices-Processing time and a maximum frequency ofoperation, memory footprint, etc.
- Performance comparison with DSPs and Multi-core SoCs.

### Learning Outcomes:

After successful completion of the module, the students shall be able

- Create their own IP and SoC design for FPGA implementation
- Perform in-system Hardware-debugging of the post-implemented design
- Develop their own software application with Zynq APSoC

### Reading List

1. K. K. Parhi, VLSI Digital Signal Processing, Wiley 1999
2. DSP Integrated Circuits, L. Wanhammar
3. Image Processing Methods - How To Develop Image Processing Systems Using Xilinx FPGA: Using A Zynq, Herman Sheroan, 2021
4. Exploring Xilinx FPGA And Heterogeneous SoC - The Principles Behind Image-Processing Sensors: Introduction To Image Processing, Synthia Collums, 2021
5. Pedroni, Volnei A., Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press,ISBN-10: 0262014335 | ISBN-13: 978-0262014335

## ES 609: Project Work/OJT

### Module Duration: 210 Hours

**Description:** The students can select hardware, software or system level projects. The project can be implemented using FPGAs, Microcontrollers, Open Source Hardware Platforms and Embedded Operating Systems which students have studied and used during the course.