PG Program in VLSI SoC Design and Verification

Course Structure*

Module Code*	Module Name	Duration (Hrs)			Credit
		Total	Theory	Lab	
VS 501	Embedded C and ARM Cortex Microcontrollers	65	13	52	3 (1+2)
VS 502	VLSI Fundamentals	65	13	52	3 (1+2)
VS 503	FPGA Architecture and Programming using Verilog HDL	65	13	52	3 (1+2)
VS 504	ARM based SoC Design	65	13	52	3 (1+2)
VS 505	Advanced ARM SoC Design	65	13	52	3 (1+2)
VS 506	SoC Verification	65	13	52	3 (1+2)
VS 507	Project	210		210	8
	Total	**600**	**78**	**522**	**26**

*These programs are conducted as workshops/ internship. Modular admission is available and those who are completing all the modules are eligible for PG Program in VLSI SoC Design and Verification on production of the Provisional Degree Certificate of B.E./B.Tech.

Course Preamble:

The complex Very Large Scale Integrated (VLSI) systems are built on System on Chips (SoCs). In a SoC usually, many processor cores and the essential peripherals are wrapped. To design a SoC, knowledge in processor architectures, various bus protocols, etc. are essential. Also, the SoC verification is more challenging as it involves the verification of many complex scenarios. Therefore usually the SoCs are emulated on a Field Programmable Gate Array (FPGA) and the real chip verification will be carried out before spin.

This VLSI SoC Design and Verification course focus on building the necessary industry skills required to work in SoC Design/Verification/FPGA Emulation projects. The course focus on industry-standard Advanced RISC Machine (ARM) processors based SoC design, verification, and FPGA emulation. The necessary skills (Verilog HDL Coding for synthesis, FPGA

Architecture and programming, System Verilog based Verification, etc.) required to fetch an industry job are covered in this course. The course will transform the successful participants into industry-ready employable engineers. In addition, it helps to hand-hold startup industries in the VLSI SoC Design/Verification/Emulation domain.

Objective of the Course

PG Program in VLSI SoC Design and Verification Course is intended to impart skills essential for VLSI Circuits design, ARM based SoC design, Verification, Software programming.

Outcome of the Course:

The successful participants will have;

1. In-depth knowledge, skills and comprehensive understanding about the Electronics fundamentals, SoC Design and Verification methodologies and industry practices followed by VLSI Design Companies across the world.
2. Ready employability in multiple roles available in VLSI Industry.
3. Refined skillsets, knowhow and confidence needed for entrepreneurship in VLSI Design and Verification industry.

Duration: 600 Hours

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.
However, they will be issued course certificate only on production of their provisional/degree certificate

VS 501: Embedded C and ARM Cortex Microcontrollers

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

This module aims at familiarizing the students in embedded concepts, programming in 'C' and ARM Architecture. This module covers the introduction to embedded systems and advanced topics in 'C' such as Memory management, Pointers, Data structures which are of high relevancein embedded software is considered in depth. This module also covers the Architecture of ARM and application development with ARM Cortex Microcontrollers.

Learning Outcomes

After successful completion of the module, the students shall be able to understand:

- Development of Embedded applications using Embedded C
- Usage of ARM Cortex Microcontrollers with Embedded C Programming for Application Development

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Prerequisite: NIL

Course Description

Embedded Concepts

Introduction to embedded systems, Application areas and categories of embedded systems, Overview of embedded system architecture, Specialties and trends in embedded systems, Development and debugging Tools.

'C' and Embedded C

Introduction to 'C' programming, Storage Classes, Data Types, Controlling program flow, Arrays, Functions, Memory Management, Pointers, Arrays and Pointers, Pointer to Functions and advanced topics on Pointers, Structures and Unions, Data Structures, Linked List, Stacks, Queues, Conditional Compilation, Preprocessor directives, File operations, Variable arguments in Functions, Command line arguments, bitwise operations.

Introduction to ARM Cortex Architecture

Introduction to ARM Architecture, Overview of ARM, Overview of Cortex-M Architecture

Cortex M3 Microcontrollers & Peripherals

Cortex M3 based Microcontroller architecture, Memory mapping, ARM Cortex M3 Peripherals – GPIOs, Timers, UARTs, Cortex M3 interrupt handling (NVIC), ARM Cotex-M3 Programming and application development.

Reading List

Text Books:

1. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
2. Let us C by Yashwant Kanetkar.
3. The Definitive Guide to the ARM Cortex M3, Joseph Yiu, Newnes.

Reference Books:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill.
2. Embedded C, Pont, Michael J
3. Embedded Systems an Integrated Approach: Lyla B Das, Pearson
4. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
5. Art of C Programming, JONES, ROBIN,STEWART, IAN
6. ARM System Developer's Guide - Designing and Optimizing System Software by: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elsevier.
7. ARM Cortex M3 Reference manual.
8. STM32Ldiscovery datasheets, reference manuals & Application notes.

VS 502: VLSI Fundamentals

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

The objective of the course is to give students solid introductory knowledge on VLSI design and the application of these concepts.

Learning Outcomes

On successful completion of the module, the candidate shall be able to:

- Get an overview of VLSI Design, its importance in the electronics industry, and its applications.

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Course Description

Introduction to VLSI
Introduction to VLSI Design Flow: Front-end and Back-end, Industry standard VLSI Design Tools. CMOS transistor theory, CMOS inverter characteristics, Fabrication steps of a CMOS inverter.

Circuits and Layout
Transistor level schematics and layouts for: CMOS inverter, NAND, NOR Gates, D-Flip Flop, D-Latch. On chip wire modelling. Bonding diagram, packaging and assembly.

Timing in VLSI circuits
Gate Delays and Logical effort. Combinational logic circuit critical path optimization. Usage of P/N ratio to determine the best delay/power trade-off for logic gates. Timing in sequential circuits, timing constraints, maximum frequency of operation, techniques to improve timing.

Processor Architecture and Design for Testability
Introduction to processor architectures. Data path and Control path Design, Design of a simple processor.

Stuck at fault model, Generation of test vectors to find stuck at faults, scan chains, Introduction to BIST, IEEE boundary scan methodology.

Reading List

1. Digital Integrated Circuits - A design perspective: JAM M RABEY
2. CMOS VLSI Design: A Circuits and Systems Perspective-Book by David Harris and Neil Westes
3. Digital Design and Computer Architecture-Book by David Harris
4. Digital VLSI Chip Design with Cadence and Synopsys CAD Tools-Book by Erik Brunvand

VS 503: FPGA Architecture and Programming using Verilog HDL

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

The objectives of the course is to:

1. Provide a thorough understanding about and hands-on with digital design & Test bench based verification using Verilog HDL.
2. Provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation**.**

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Author Design IPs for VLSI using Verilog HDL
- Develop Test benches using Verilog HDL
- Prototype digital Systems using FPGA
- Emulate, debug & Characterize reusable IPs

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Prerequisite: Completion of module VS 501

Course Description

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Gate Level Modeling
- Dataflow Modeling
- Behavioural Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow - Xilinx Vivado®

- Logic Synthesis and timing for FPGA
- IP Core based Design
- Debugging using Embedded Logic Analyzers
- Design problems using Xilinx® Platforms
- Case Studies on FPGA Based implementations
- Mini-project and Case Studies

Reading List

1. Verilog HDL - A guide to Digital Design and Synthesis by Samir Palnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi
5. FPGA-Based System Design by Wayne Wolf
6. Advanced FPGA Design Architecture, Implementation and optimization by Kilts
7. Embedded Core Design with FPGAs. by Zainalabedin Navabi
8. FPGA Prototyping by Verilog Examples by Pong P. Chu
9. Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL by Michael D. Ciletti

VS 504: ARM based SoC Design

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

The objective of the course is to provide a thorough understanding about and hands-on practice with ARM based SoC design and emulation using FPGA.

Learning Outcomes

After successful completion of this module, students should be able to:

- Prototype a SoC on FPGA
- Perform low-level software design for Arm-based SoCs and high-level application development
- Acquire ability to use a commercial tools to develop Arm-based SoCs

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Prerequisite: Completion of module VS 503

Course Description

- Introduction to Programmable SoCs
- AHB Light bus architecture
- Building a System on Chip- Integrating AHB peripherals to ARM
    - UART
    - Timer,GPIO
    - Interrupt Controller
- Software Programming of ARM SoC

Reading List

1. ARM System-on-Chip Architecture by Steve B. Furber
2. ARM Assembly Language: Fundamentals and Techniques by William Hohl
3. The Definitive Guide to the ARM Cortex-M0 by Joseph Yiu

VS 505: Advanced ARM SoC Design

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

The objective of the course is to

- Provide understanding about developing ARM SoCs from creating high level functional specifications to design, implementation and testing on FPGA platforms using standard hardware description and software programminglanguages.

students who are capable of developing Arm Cortex-A based SoCs, from creating high level functional specifications to design, implementation and testing on FPGA platforms using standard hardware description and software programming languages

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Development of ARM SoCs on FPGA and development of applications.

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Prerequisite: Completion of module VS 503, VS 504

Course Description

- ARM SoCs (Arm Cortex-A series)
- AXI Bus Architecture
- Design of ARM based advanced SoCs

- Integrating AXI Peripherals to ARM SoC

Reading List

1. ARM System-on-Chip Architecture by Steve B. Furber
2. ARM Assembly Language: Fundamentals and Techniques by William Hohl
3. Cortex-A Series Programmer's Guide for ARMv7-A by Arm http://infocenter.arm.com/help/topic/com.arm.doc.den0013d/index.html
4. GNU/LINUX Application Programming, Jones, M Tims
5. Embedded Linux: Hardware, Software, and Interfacing, Hollabaugh, Craig,
6. Building Embedded Linux Systems: Yaghmour, Karim
7. Embedded/Real-Time Systems: Concepts, Design and Programming: The Ultimate Reference, Dr. K.V.K.K. Prasad, Published by Wiley DreamTech, 2003
8. ARM System Developer's Guide - Designing and Optimizing System Software by: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elseiver.
9. FPGA-Based System Design by Wayne Wolf
10. Advanced FPGA Design Architecture, Implementation and optimization by Kilts

VS 506: SoC Verification

Module Duration: 65 Hours (13 hours theory and 52 hours lab)

Objective

The objective of the course is to provide understanding of the techniques for SoC Verification

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Perform design verification of SoCs using System Verilog

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS).

or

Ongoing with 3rd semester completed.

Prerequisite: Completion of module VS 504, VS 505

Course Description

- Introduction to VLSI Verification-Verification Architecture, Test automation, Assertions and Coverage.
- System Verilog Features
- Basic Data Types
- Operators
- Bus Function Modeling
- Interfaces, RTL Processes
- Clocking Blocks
- Randomization, Coverage
- Arrays & Queues
- Direct Programming Interface
- Monitors & Checkers
- Functional Coverage
- Processes and Events

- Verification of SoC
- Verification Planning & Challenges

Reading List

1. Writing Testbenches: Functional Verification of HDL Models by Janick Bergeron
2. SystemVerilog for Verification by Chris Spear
3. System Verilog for Design by Chris Spear
4. RTL Modeling with SystemVerilog for Simulation and Synthesis by Stuart Sutherland
5. System Verilog Assertions and Functional Coverage by Mehta
6. Logic Design and Verification Using SystemVerilog by Donald Thomas
7. Designing Digital Systems With SystemVerilog by Brent E. Nelson

Standard

"IEEE Standard for System Verilog-Unified Hardware Design, Specification, and Verification Language," in IEEE Std 1800-2017, vol., no., pp.1-1315, 22 Feb. 2018, doi: 10.1109/IEEESTD.2018.8299595.Available online at https://ieeexplore.ieee.org/document/8299595

VS 507: Project Work

Module Duration:210 Hours

Objective:

The objective of project work is to demonstrate the candidates' skill and knowledge in solving a real work Engineering problem involving VLSI Design or Verification.

Learning Outcomes

After successful completion of this module, the candidate shall be able to:

- Undertake and indecently complete a real world Industry problem involving VLSI Design or Verification using state of the art industry standard tools and practices

Target Audience: B.E./B.Tech./MCA/BCA/NIELIT A Level Completed or Ongoing with 3rd semester completed.

Prerequisite: Completion of modules relevant to the chosen project problem.

Description

The participants can choose projects involving one among the following;

RTL Design, ARM Based SoC Design, Verification, ARM Based SoC Applications, etc.