COURSE PROSPECTUS

Name of the Group: *VLSI Lab- Smart Technology and Education Division*
Name of the Course: *Certificate Program in VLSI Physical Design*
Course Code: *VL702*
Duration: *3 Months.*
Starting Date: *13-01-2025*
Course Coordinator: *Sreejeesh SG- 9447769756*
Co-Coordinator: *Nandakumar R -9995427802*

Preamble: VLSI (Very Large Scale Integration) has emerged as a very significant technology to provide tremendous quantum of process technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvements in performance while achieving reduction in the size, cost and power consumption. Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.

In today's world, Embedded Systems are all over homes, offices, cars, factories, hospitals, and Industries. The inherent value of these technologies lies in their pervasiveness. They are literally embedded in all electronic products, from consumer electronics to office automation, automotive, medical devices, and communications. They make the products smart, connected and are responsible for differentiating the products in the market.
Developing tomorrow's industrial infrastructure is a significant challenge. This course goes beyond the hype of consumer IoT to emphasize a much greater space for potential embedded system applications and growth. The primary objective of this specialization is to closely examine emerging markets, technology trends, applications, and skills required by engineering students or working engineers, exploring career opportunities in the Embedded System design and IoT space.

Objective of the Course:

It is proposed to offer Certificate Program in VLSI Physical Design to enable new Electronics graduates/post graduates or working engineers in electronic industries to the concepts used in IC Design, which involves processing, Layout, System Design Methods using Cadence tool. The course will benefit VLSI Engineers seeking lateral shift to a back end job. Engineers looking to work for Block level Physical Design Implementation, Place and Route job domains. This will take VLSI Engineers to a new level known as Physical Design Engineer. The Physical Design Engineer is responsible for converting the circuit design to a geometric representation for manufacturing the integrated circuit (IC).

The main objective of the course is to make individuals understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout

During course work, each individual will get ample time to practice the theory taught in class in the lab sessions.

Outcome of the Course: After successful completion of the course individuals will understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout. The course will also help to fetch VLSI Physical Design job for job seekers in VLSI area.

Course Structure:

VL702	Module name	Duration
Module 1	*RTL Design using Verilog HDL*	*4 Weeks*
Module 2	*Digital Physical Design Flow*	*4 Weeks*
Module 3	*Project*	*4 Weeks*

Other Contents

I. **Course Fees**: **Course fee** is ₹*35,000*/- inclusive all taxes

II. **Registration Fee:** An amount of ₹1000/- (including all taxes as applicable) (nonrefundable) should be paid at the time of registering for the course.

This fee shall be considered as part of course fee, if the student joins the course. If the student does not join for the course fee paid shall be forfeited.

However above the registration fee shall be refunded for all category students on few special cases as given below

- Course postponed and new date is not convenient for the student
- Course canceled in advance, well before the admission date

III. **Course Fee Installment Structure**:

Students can pay the full fees of ₹. *35000/- (inclusive of all taxes)* in advance or as installments as given below

Fees	Amount *	Due Date (on or before) #
Registration Fee	₹1000/-	During Registration
**Advance Fee	₹*4000/-*	*06-01-2025*
1st Installment	₹*15,000/-*	*13-01-2025*
*** 2nd Installment	₹*15,000/-*	*13-02-2025*
Total Fee	₹*35,000/-*	*13-02-2025*

*Above fees is inclusive *CGST* 9% and SGST 9%, and revision, if any by Government shall be applicable at the time of payment.

Fine will be applicable for late fee payment.

** Advance fee - After publication of first selection list, the selected students have to pay the Advance Deposit within the due date to take the provisional admission. Students in the additional selection list should pay both Advance and First installment fee together on or before counseling day

IV. Eligibility: M.E/ M.Tech/ B.E/ B.Tech/ M.Sc in Electrical/ Electronics and Communication/ Electronics and Instrumentation/ Computer Science and allied branches./ M.Sc (Electronics/CS).

Graduates with appropriate experience and final year students# also may apply. # Final year students have to include the copies of course completion certificate of their qualifying degree/ diploma or copies of the mark lists up to the last semester/ year. On the date of counseling/ admission, he/she must produce the originals of course completion certificate/ mark lists up to the last semester/year examination.

V. Number of Seats : *15*

VI. Selection of candidates: Based on marks obtained in the respective degree course as per eligibility.

NB: ***Students are requested to bring laptops***

VII. Test/Interview : *Not Applicable*

VIII. Counseling/Admission : 13-01-2025

IX. Important Dates:

Publication of Selection List in Institute Website: *01-01-2025*
Advance Fee Payment (on or before): *06-01-2025*
Counseling: *13-01-2025*
Starting Date*: 13-01-2025*

X. Course Timings : *10:00am to 4:00 pm*

XI. Placement : *http://nielit.gov.in/content/placement-3*

XII. Lab Facilities : *http://nielit.gov.in/calicut/calicut/content/vlsi-design-group*

Module 1: System Design using Verilog HDL – One Month

Introduction to Verilog HDL & Hierarchical Modeling Concepts, Lexical Conventions & Data Types, System Tasks & Compiler Directives, Modules, Ports and Module Instantiation Methods, Gate Level Modeling, Dataflow Modeling, Behavioral Modeling, RTL Design and Logic Synthesis and Synthesis issues, design Verification using Test benches, Mini-project and Case Studies

Module 2: Digital Physical Design Flow- One Month

ASIC Design Concepts, ASIC Design Flow-Frontend and backend, EDA tools for Frontend and backend, Introduction to Verilog HDL, Hardware Modeling Overview

a) ***Digital ASIC Design Synthesis:*** Introduction to Digital Synthesis: Synthesize a block-level RTL design to generate a gate-level netlist using Cadence Synthesis Tool.
b) ***Physical Design Flow Setup and Floorplan*** List of inputs (libraries, technology files, netlist, timing constraints, and IO placement) to the PD flow, contents of each input, qualifying the received inputs and sanity checks. Goals of floor planning, different aspects of floor planning, Area estimation, Square/Rectangle/Rectilinear Floorplans, IO placement, macro placement, channel-width estimation, Floor planning guidelines.
c) ***Power Routing & Placement:*** Goals of Power Routing, Types of Power Routing, PG-Rings, PG Mesh and follow-pin/Std cell rail. Goals of Placement, types of placements, pre-place (End-cap, Tap & I/O Buffer) cells, pre-place optimization and in-place optimization, congestion analysis, timing analysis.
d) ***Timing Analysis & Optimization:*** Basic timing checks in digital circuits like Setup Time Violations and Hold Time Violations, understanding timing constraints, timing corners, timing report analysis, general optimization techniques, and typical causes for timing violations and strategies for fixing the same.
e) ***Clock Tree Synthesis (CTS) & Routing:*** What is Clock Tree Synthesis and its Goals, Types of Clock-tree, CTS Specification, Building clock tree, analyze the results, Fine-tuning the Clock-tree and Guidelines for best CTS results. Goals of Routing, Types-of Routing, Global Routing, Detail Routing, Fixing of routing violations (DRC, LVS), and post route optimization.
f) ***ECO Flow & Sign-off Checks:*** What is ECO, Types of ECO, Timing & Functional ECO prep, rolling in the ECO, Performing the ECO placement and routing. Physical Verification (DRC, LVS, ERC), Sign-off Timing analysis.

Project- One Month

One projects should be taken up covering RTL to GDS flow. We will adopt the industry standard flow for the implementation.

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