COURSE PROSPECTUS

**Name of the Group:** *STED*
**Name of the Course:** *PG Program in VLSI & Embedded System Design*
**Course Code:** *VESD-500*
**Duration:** *24 Weeks.*
**Starting Date:** *23-09-2024*
**Course Coordinator:** *Sreejeesh SG / Sri Rama Pavan :* ***9447769756/8904310403***

**Preamble:** *VLSI (Very Large Scale Integration) has emerged as a very significant technology to provide tremendous quantum of process technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in some dramatic improvements in performance while achieving reduction in the size, cost and power consumption. Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.*

*In today's world, Embedded Systems are all over homes, offices, cars, factories, hospitals, and Industries. The inherent value of these technologies lies in their pervasiveness. They are literally embedded in all electronic products, from consumer electronics to office automation, automotive, medical devices, and communications. They make the products smart, connected and are responsible for differentiating the products in the market.*

*Developing tomorrow's industrial infrastructure is a significant challenge. This course goes beyond the hype of consumer IoT to emphasize a much greater space for potential embedded system applications and growth. The primary objective of this specialization is to closely examine emerging markets, technology trends, applications, and skills required by engineering students or working engineers, exploring career opportunities in the Embedded System design and IoT space.*

**Objective of the Course:** *This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by Embedded & VLSI markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices.*

- *This uniquely hybrid course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries. For people interested in entrepreneurships this would be an excellent launch pad. In addition the course also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.*

- *Provide the participants in-depth knowledge and skills required by Embedded System companies around the globe by imparting comprehensive understanding about the fundamental principles, methodologies and industry practices.*
-

- *Makes the successful participants readily employable in multiple roles available in Embedded and enhances the skillsets and confidence for Embedded Startups.*

**Outcome of the Course:** *Outcome of the Course*

**Course Structure:** *The VESD500 contains Nine modules. The students are required to do a project work in any one of the modular areas, for a period of 7 weeks to be eligible for issue of PG Program in VLSI & Embedded System Design*

| Module No | *Module Name* | Duration(Weeks) |
|---|---|---|
| 1. | *Advanced Digital Design* | *1* |
| 2. | *CMOS Logic Design* | *1* |
| 3. | *Embedded C and ARM Cortex Microcontrollers* | *4* |
| 4. | *Embedded Linux* | *2* |
| 5. | *Embedded RTOS* | *2* |
| 6. | *Verilog HDL : Language and Coding for Synthesis* | *2* |
| 7. | *FPGA Design Methodology and Prototyping* | *3* |
| 8. | *Embedded Product Design* | *2* |
| 9. | *Project Work* | *7* |
| | **Total Duration** | ***24*** |

*Other Contents*

**I. Course Fees**: **Course fee** is ₹ *70,000*/- inclusive of all taxes

**II. Registration Fee:** An amount of ₹.1000/- (including all taxes as applicable) (nonrefundable) should be paid at the time of registering for the course.

This fee shall be considered as part of course fee, if the student joins the course. If the student does not join for the course fee paid shall be forfeited.

However above the registration fee shall be refunded for all category students on few special cases as given below

- Course postponed and new date is not convenient for the student
- Course canceled in advance, well before the admission date

**III. Course Fee Installment Structure**:
(*applicable only to PG/Advanced Diploma courses. For all other courses may be indicated as* "Not applicable for this course")

Students can pay the full fees of ₹ *70000/- (inclusive of all taxes)* in advance or as installments as given below

| Fees | Amount * | Due Date (on or before) # |
|---|---|---|
| Registration Fee | ₹.1000/- | During Registration |
| **Advance Fee | ₹.*9000/-* | *16-09-2024* |
| 1st Installment | ₹.*30,000/-* | *23-09-2024* |
| *** 2nd Installment | ₹.*30,000/-* | *23-12-2024* |
| Total Fee | ₹.*70,000/-* | *23-12-2024* |

*Above fees is inclusive *CGST* 9% and SGST 9%, and revision, if any by Government shall be applicable at the time of payment.

# Fine will be applicable for late fee payment.

** Advance fee - After publication of first selection list, the selected students have to pay the Advance Deposit within the due date to take the provisional admission. Students in the additional selection list should pay both Advance and First installment fee together on or before counseling day

**IV.** Eligibility: M.E/M.Tech/B.E/B.Tech(ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc (Electronics/CS). Graduates with appropriate experience and final year students# also may apply. # Final year students have to include the copies of course completion certificate of their qualifying degree/ diploma or copies of the mark lists up to the last semester/ year. On the date of counseling/ admission, he/she must produce the originals of course completion certificate/ mark lists up to the last semester/year examination

**V.** Number of Seats : *20*

**VI.** Selection of candidates : Selection will be based on the marks secured in the qualifying *exam*

**VII.** Test/Interview (*if applicable*) : Not applicable

**VIII.** Counseling/Admission: *23-09-2024*

***IX.*** Important Dates (if applicable) :

Publication of Selection List in Institute Website 10-09-2024
Advance Fee Payment (on or before):16-09-2024
Counseling: 23-09-2024

**X.** Course Timings : *10:00am to 4:30 pm*

**XI.** Placement : *http://nielit.gov.in/content/placement-3*

**XII.** Lab Facilities : *http://nielit.gov.in/calicut/calicut/content/vlsi-design-group*
*https://nielit.gov.in/calicut/content/embedded-system-group*
*https://nielit.gov.in/calicut/calicut/content/product-engineering-group*

Course Contents: **Module 1: Advanced Digital Design (1 Week)**

- Combinational Circuit Design
- Sequential Circuit Design
- Design of controller and Data path units
- State Machines
- Controller Design using FSMs & ASMs
- Design Examples & Case Studies

**Module 2: CMOS Logic Design (1 Week)**

- MOS Fundamentals,
- MOS Switches & Designs
- Transmission Gates,
- Inverter - DC, AC Characteristics,
- Combinational and Sequential Logic,
- Introduction to Layout Tools

**Module 3: Embedded C and ARM Cortex Microcontrollers (4 Weeks)**

- Introduction to Embedded Systems
- Embedded C Programming
- ARM Cortex M Architecture Overview
- Introduction to STM32 Microcontrollers & Development Boards
- Overview of IDEs for STM32 Microcontrollers
- Peripheral libraries & drivers for STM32 Microcontrollers
- Sensors and actuators interfacing with STM32 Microcontrollers
- Serial & Bus protocols with STM32 Microcontrollers
- Mini Project

**Module 4: Embedded Linux (2 Weeks)**

- Introduction to Embedded Systems and Linux
- System architecture of Embedded Linux OS
- Configuration & Build Process of an Embedded Linux System
- Linux Kernel Modules
- Application Demo: Building a custom Kernel Module

**Module 5: Embedded RTOS (2 Weeks)**

- Introduction Real Time Systems and RTOS
- System architecture of FreeRTOS/RTX
- System architecture of Real Time Linux/ VxWorks.

**Module 6: Verilog HDL: Language and Coding for Synthesis (2 Weeks)**

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives

- Modules, Ports and Module Instantiation Methods
- Gate Level Modeling
- Dataflow Modeling
- Behavioral Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Mini-project and Case Studies

**Module 7: FPGA Design Methodology and Prototyping (3 Weeks)**

- Introduction to Programmable Logic and FPGAs
- Popular FPGA Families
- Architecture of popular Xilinx
- FPGA Design Flow using Vivado
- Implementation Details.
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Design problems using Xilinx Platforms
- Case Studies on FPGA Based implementations

**Module 8: Embedded Product Design (2 Weeks)**

- Product Development Process
- Detailed Engineering design
- Electronic Circuit Design
- Semiconductor Packages
- Printed circuit board Design
- High Speed PCB Design
- Hardware Testing & Software testing tools
- PCB Assembly process (DFM, DFA etc)
- Certification and regulatory requirements.

**Module 9: Project Work**

Click here for General Terms and Conditions – Applicable to all courses