NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY(NIELIT) AURANGABAD

CEDTI Complex, Dr. B.A.M. University Campus Aurangabad (Ch.Sambhaji Nagar) Maharashtra-431004

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SIX MONTHS POST-GRADUATE DIPLOMA IN SYSTEM ON CHIP DESIGN AND VERIFICATION

Course Prospectus & Detailed Curriculum

COURSE PROSPECTUS

Name of the Department: *Electronics*

Name of the Course: *PG Diploma in System on Chip Design and Verification*

Course Code: *SDV 500*

Starting Date: *19 Aug 2024*

Duration: *24 Weeks (720 Hours)*

Course Coordinator : Shri. *Sourabh Kesari, 91-7386929670,* saurabhk@nielit.gov.in
Co-Coordinator : Shri. *Shashank Kumar Singh*, 91-9999026637, shashank@nielit.gov.in

Course Preamble:

Complex Very Large Scale Integrated (VLSI) systems are typically constructed on System on Chips (SoCs). Within an SoC, multiple processor cores and essential peripherals are commonly integrated. Designing an SoC necessitates expertise in processor architectures, diverse bus protocols, and related areas. Moreover, verifying an SoC presents significant challenges due to the multitude of complex scenarios involved. Consequently, SoCs are often emulated on Field Programmable Gate Arrays (FPGAs) to facilitate verification, with final chip verification conducted prior to fabrication.

This SoC Design and Verification course is tailored to equip participants with the essential industry skills needed for roles in SoC Design, Verification, and FPGA Emulation projects. It specifically emphasizes industry-standard RISC processor-based SoC design, verification, and FPGA emulation. Key skills such as Verilog HDL Coding for synthesis, FPGA Architecture and programming, and System Verilog-based Verification are comprehensively covered, ensuring participants are well-prepared for employment in the industry. Successful completion of the course will transform participants into professionals who are immediately employable in the field. Furthermore, it provides valuable support to startup industries operating in the SoC Design, Verification, and Emulation domain.

Objective of the Course

The PG Diploma in SoC Design and Verification Course aims to provide comprehensive training in key skills vital for various aspects of VLSI Circuits design, including RISC Processor-based SoC design, Verification, Embedded Software development, OS porting, and application building.

Outcome of the Course:

The successful participants will have;

1. Gain extensive knowledge, skills, and a thorough understanding of Electronics fundamentals, SoC Design, and Verification methodologies, along with insight into industry practices adopted by VLSI Design Companies globally.
2. Attain readiness for employment across various roles within the VLSI Industry, equipped with the necessary expertise and competencies.
3. Develop refined skill sets, knowledge, and confidence essential for entrepreneurial endeavours within the VLSI Design and Verification industry, fostering the capability to establish and manage ventures successfully.

Expected job roles

- SoC Design Engineer
- Verification Engineer
- ASIC Design Engineer
- FPGA Design Engineer
- Verification and Validation Engineer
- System Architect
- RTL Design Engineer

Course Structure

Module Code	Module Name	Duration (Hrs)			Credits
		Total	Theory	Practical	
SDV 500	VLSI Fundamentals	45	15	30	2 (1+1)
SDV 501	Embedded C and ARM Cortex Microcontrollers	90	30	60	4 (2+2)
SDV 502	FPGA Architecture and Programming using Verilog HDL	45	15	30	2 (1+1)
SDV 503	RISC processor based SoC Design	90	30	60	4 (2+2)
SDV 504	Advanced SoCs and OS Porting	45	15	30	2 (1+1)
SDV 505	SoC Verification	90	30	60	4 (2+2)

SDV 506	Industrial Training and Employability Skills	75		75	
SDV 507	Project	240		240	26
	Total	**720**	**135**	**585**	**26**

Duration: 720 Hours

Course Fees: Rs. 60,000/- + GST and other taxes if any as applicable

Registration fee: An amount of Rs.1000/- (including all taxes as applicable) (nonrefundable) should be paid at the time of registering for the course.

This fee shall be considered as part of course fee, if the student joins the course. If a student register and pay for more than one course and join for any one course, all such amount will be adjusted against the course fee payable.

If the student does not join for the registered course / any of the registered courses, fee paid shall be forfeited.

Course Fee Installment Structure:

Students can pay the full fees of Rs. *60,000 + all taxes as applicable* (Rs. 70,800/-)in advance or as installments as given below.

Fee	Amount in Rs.	# Due date
Registration Fee	1,000/-	
**Advance Fee	10,000/-	
1st Installment	35,000/-	
2nd Installment	24,800/-	
Total fee	70,800/-	

**Advance fee – After publication of first selection list, the students in the first selection list have to pay the Advance Deposit within the due date to take the provisional admission. Students in the additional selection list should pay both Advance and First installment fee together on or before counseling day.

Fine will be applicable for late payment.

Eligibility: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS) Completed or *Final Year, NIELIT 'A' Level.

* Upon fulfilling all requirements, final year students will receive a PG Diploma certificate alongside their degree. Submission of proof of degree completion is necessary to obtain the PG Diploma certificate; otherwise, a course completion certificate will be provided.

Number of Seats : ***40***

Selection of candidates :

The selection to the course shall be based on the following criteria:

i. Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

ii. The First list of Provisionally Selected Candidates will be intimated on ***15/07/2024*** *by email only. In case of vacancy, additional selection list will be prepared and the selection will be intimated by email only.*

iii. All candidates who appear in the first selection list may pay Rs.10,000/- *on or before* ***22nd July 2024*** *by* ***direct payment into our account*** *from any bank where core banking facility is available. Selected candidates are requested to send the proof of remittance of fee as email, so as to reach the center by* ***25th Aug 2024.***

Test/Interview: *Not Applicable*

Counselling/Admission:

All candidates ***provisionally selected*** *and* ***paid the advance fee*** *will have to be present personally for* ***counseling and admission on 20th or 21th Aug 2024*** *with all the necessary documents (originals and attested copies). Working days are from Monday to Friday. Admission timings are from 9.30 am to 4.00 pm.*

Important Dates:

Date	
15th May 2024	**Course Registration opens**
15st July 2024	**First election List**
22th July 2024	**Last date for paying the advance fee**
29th July 2024	**Second selection list**
19th & 20th Aug 2024	**Counselling and admission**
21st Aug 2024	**Commencement of classes**

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The classes and labs are from 9.30 am to 12.45 pm and 1.30 pm to 5.15 pm Monday to Friday. During project work, the timings are from 9.15 am to 5.15 pm. The theory to lab proportion is 30:70.

Placement:

We have a placement cell, which provides placement assistance to students who qualify our courses. Internship/Placement/Entrepreneurship support also will be provided under ***Chips to Start up*** *(***https://www.c2s.gov.in) programme of Ministry of Electronics and Information Technology, GoI.**

The course improves the knowledge and skill of the students as it deals with the latest technologies and tools used in industries. This helps the student in getting a placement by

i. Campus placement

ii. Placement by companies for whom we send the students bio data and they conduct interviews at their site.

iii. Students themselves attend interview at different companies and the course helps in the interview.

Lab Facilities *: NIELIT Aurangabad is a participating institute under C2S Programme of MeitY along with other elite 100 institutions across the country. The VLSI, FPGA and SoC Design Labs are equipped with Industry standard VLSI Design tools from Synopsys, CADENCE, AMD (Xilinx) and SIEMENS-Mentor.*

Detailed Curriculum & Syllabus:-

SDV 500: VLSI Fundamentals

Module Duration: 45 Hours (15 hours theory and 30 hours lab)

Objective

The objective of the course is to give students solid introductory knowledge on VLSI design and the application of these concepts.

Learning Outcomes

On successful completion of the module, the candidate shall be able to:

- Get an overview of VLSI Design, its importance in the electronics industry, and its applications.

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level..

Prerequisite: Knowledge in Analog and Digital Circuit Design basics

Course Description

Introduction to VLSI
Introduction to VLSI Design Flow: Front-end and Back-end, Industry standard VLSI Design Tools. CMOS transistor theory, CMOS inverter characteristics, Fabrication steps of a CMOS inverter.

Circuits and Layout
Transistor level schematics and layouts for: CMOS inverter, NAND, NOR Gates, D-Flip Flop, D-Latch. On chip wire modelling. Bonding diagram, packaging and assembly.

Timing in VLSI circuits
Gate Delays and Logical effort. Combinational logic circuit critical path optimization. Usage of P/N ratio to determine the best delay/power trade-off for logic gates. Timing in sequential circuits, timing constraints, maximum frequency of operation, techniques to improve timing.

Processor Architecture and Design for Testability
Introduction to processor architectures. Data path and Control path Design, Design of a simple processor.

Stuck at fault model, Generation of test vectors to find stuck at faults, scan chains, Introduction to BIST, IEEE boundary scan methodology.

Reading List

1. Digital Integrated Circuits - A design perspective: JAM M RABEY
2. CMOS VLSI Design: A Circuits and Systems Perspective-Book by David Harris and Neil Westes
3. Digital Design and Computer Architecture-Book by David Harris
4. Digital VLSI Chip Design with Cadence and Synopsys CAD Tools-Book by Erik Brunvand

SDV 501: Embedded C and ARM Cortex Microcontrollers

Module Duration: 90 Hours (30 hours theory and 60 hours lab)

Objective

This module aims at familiarizing the students in embedded concepts, programming in 'C' and ARM Architecture. This module covers the introduction to embedded systems and advanced topics in 'C' such as Memory management, Pointers, Data structures which are of high relevance in embedded software is considered in depth. This module also covers the Architecture of ARM and application development with ARM Cortex Microcontrollers.

Learning Outcomes

After successful completion of the module, the students shall be able to understand:

- Development of Embedded applications using Embedded C
- Usage of ARM Cortex Microcontrollers with Embedded C Programming for Application Development

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level.

Prerequisite: Programming knowledge

Course Description

Embedded Concepts

Introduction to embedded systems, Application areas and categories of embedded systems, Overview of embedded system architecture, Specialties and trends in embedded systems, Development and debugging Tools.

'C' and Embedded C

Introduction to ‘C’ programming, Storage Classes, Data Types, Controlling program flow, Arrays, Functions, Memory Management, Pointers, Arrays and Pointers, Pointer to Functions and advanced topics on Pointers, Structures and Unions, Data Structures, Linked List, Stacks, Queues, Conditional Compilation, Preprocessor directives, File operations, Variable arguments in Functions, Command line arguments, bitwise operations.

Introduction to ARM Cortex Architecture

Introduction to ARM Architecture, Overview of ARM, Overview of Cortex-M Architecture

Cortex M3 Microcontrollers & Peripherals

Cortex M3 based Microcontroller architecture, Memory mapping, ARM Cortex M3 Peripherals – GPIOs, Timers, UARTs, Cortex M3 interrupt handling (NVIC), ARM Cotex-M3 Programming and application development.

Reading List

Text Books:

1. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
2. Let us C by Yashwant Kanetkar.
3. The Definitive Guide to the ARM Cortex M3, Joseph Yiu, Newnes.

Reference Books:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill.
2. Embedded C, Pont, Michael J
3. Embedded Systems an Integrated Approach: Lyla B Das, Pearson
4. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
5. Art of C Programming, JONES, ROBIN,STEWART, IAN
6. ARM System Developer's Guide - Designing and Optimizing System Software by: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elsevier.
7. ARM Cortex M3 Reference manual.
8. STM32Ldiscovery datasheets, reference manuals & Application notes.

SDV 502: FPGA Architecture and Programming using Verilog HDL

Module Duration: 45 Hours (15 hours theory and 30 hours lab)

Objective

The objectives of the course is to:

1. Provide a thorough understanding about and hands-on with digital design & Test bench based verification using Verilog HDL.
2. Provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation**.**

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Author Design IPs for VLSI using Verilog HDL
- Develop Test benches using Verilog HDL
- Prototype digital Systems using FPGA
- Emulate, debug & Characterize reusable IPs

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level.

Prerequisite: Completion of module SDV 500

Course Description

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Gate Level Modeling
- Dataflow Modeling
- Behavioural Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow - Xilinx Vivado®
- Logic Synthesis and timing for FPGA
- IP Core based Design
- Debugging using Embedded Logic Analyzers

- Design problems using Xilinx® Platforms
- Case Studies on FPGA Based implementations
- Mini-project and Case Studies

Reading List

1. Verilog HDL - A guide to Digital Design and Synthesis by Samir Palnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi
5. FPGA-Based System Design by Wayne Wolf
6. Advanced FPGA Design Architecture, Implementation and optimization by Kilts
7. Embedded Core Design with FPGAs. by Zainalabedin Navabi
8. FPGA Prototyping by Verilog Examples by Pong P. Chu
9. Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL by Michael D. Ciletti

SDV 503: RISC Processor based SoC Design

Module Duration: 60 Hours (15 hours theory and 30 hours lab)

Objective

The objective of the course is to provide a thorough theoretical understanding and hands-on practice with ARM based SoC design and emulation using FPGA.

Learning Outcomes

After successful completion of this module, students should be able to:

- Prototype a SoC on FPGA
- Perform low-level software design for Arm-based SoCs and high-level application development
- Acquire ability to use a commercial tool to develop Arm-based SoCs

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level.

Prerequisite: Completion of module SDV 502

Course Description

- Introduction to Programmable SoCs
- Parallel(AHB) Light bus architecture

- Building a System on Chip- Integrating peripherals to RISC Processor
    - UART
    - Timer, GPIO,7 segment Display
    - Interrupt Controller
    - VGA
- Software Programming of SoC

Reading List

1. ARM System-on-Chip Architecture by Steve B. Furber
2. ARM Assembly Language: Fundamentals and Techniques by William Hohl
3. The Definitive Guide to the ARM Cortex-M0 by Joseph Yiu

SDV 504: Advanced SoCs and OS Porting

Module Duration: 45 Hours (15 hours theory and 30 hours lab)

Objective

The objective of the course is to

- Provide understanding about developing ARM advanced SoCs (Arm Cortex-A series), from creating high level functional specifications to design, implementation and testing on FPGA platforms using standard hardware description and software programming languages.
- Provide understanding of the techniques essential to port Operating System on FPGA with ARM Core.

students who are capable of developing Arm Cortex-A based SoCs, from creating high level functional specifications to design, implementation and testing on FPGA platforms using standard hardware description and software programming languages

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Development of ARM advanced SoCs on FPGA and development of applications.
- Port the Linux OS on FPGA with ARM Core

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level.

Prerequisite: Completion of module SDV 502, SDV 503

Course Description

- ARM/RISC-V based SoCs
- AXI Bus Architecture
- Design of ARM based advanced SoCs
- Integrating AXI Peripherals to ARM SoC
- Linux Porting and running application
- Design an Acceleration IP (Signal/Image Processing)
- Interfacing Acceleration IP with ARM SoC and FPGA Acceleration.

Reading List

1. ARM System-on-Chip Architecture by Steve B. Furber
2. ARM Assembly Language: Fundamentals and Techniques by William Hohl
3. Cortex-A Series Programmer's Guide for ARMv7-A by Arm
   http://infocenter.arm.com/help/topic/com.arm.doc.den0013d/index.html
4. GNU/LINUX Application Programming, Jones, M Tims
5. Embedded Linux: Hardware, Software, and Interfacing, Hollabaugh, Craig,
6. Building Embedded Linux Systems: Yaghmour, Karim
7. Embedded/Real-Time Systems: Concepts, Design and Programming: The Ultimate Reference, Dr. K.V.K.K. Prasad, Published by Wiley DreamTech, 2003
8. ARM System Developer's Guide - Designing and Optimizing System Software by: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elseiver.
9. FPGA-Based System Design by Wayne Wolf
10. Advanced FPGA Design Architecture, Implementation and optimization by Kilts

SDV 505: SoC Verification

Module Duration: 90 Hours (30 hours theory and 60 hours lab)

Objective

The objective of the course is to provide understanding of the techniques for SoC Verification

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Perform design verification of complex SoCs using System Verilog

Target Audience: BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc. (Electronics/CS)/ NIELIT A Level.

Prerequisite: Completion of module SDV 503, SDV 504

Course Description

- Introduction to VLSI Verification-Verification Architecture, Test automation, Assertions and Coverage.
- System Verilog Features
- Basic Data Types
- Operators
- Bus Function Modeling
- Interfaces, RTL Processes
- Clocking Blocks
- Randomization, Coverage
- Arrays & Queues
- Direct Programming Interface
- Monitors & Checkers
- Functional Coverage
- Processes and Events
- About Processor Core & IP
- Verification of RISC provessor based SoC
- Verification Planning & Challenges
- IP Connectivity Verification
- Performance Verification

- Low Power Verification
- Clock Domain Crossing Verification
- H/W -S/W Co-Verification Steps
- Tracking Verification Utility
- Tape Out readiness guidelines
- SoC/IP Verification - A case study

Reading List

1. Writing Testbenches: Functional Verification of HDL Models by Janick Bergeron
2. SystemVerilog for Verification by Chris Spear
3. System Verilog for Design by Chris Spear
4. RTL Modeling with SystemVerilog for Simulation and Synthesis by Stuart Sutherland
5. System Verilog Assertions and Functional Coverage by Mehta
6. Logic Design and Verification Using SystemVerilog by Donald Thomas
7. Designing Digital Systems With SystemVerilog by Brent E. Nelson

Standard

"IEEE Standard for System Verilog-Unified Hardware Design, Specification, and Verification Language," in IEEE Std 1800-2017, vol., no., pp.1-1315, 22 Feb. 2018, doi: 10.1109/IEEESTD.2018.8299595.Available online at https://ieeexplore.ieee.org/document/8299595

SDV 506: Industrial Training and Employability Skills

Module Duration: 75 Hours

Objective: To empower individuals with the tools and resources they need to succeed in their chosen career paths and contribute effectively to the workforce.

Learning Outcomes

After successful completion of this module, the candidate shall be able to:

- Competence in SoC Design, Integration and Verification.
- Communicate effectively among team members.
- Collaborate and work in a team.
- Obtain leadership skills.

Target Audience: B.E./B.Tech./MCA/BCA/NIELIT A Level/M.Sc. (Electronics/CS)

Prerequisite: Completion of all SDV modules.

Description

The learning outcomes of this module collectively contribute to the holistic development of individuals, preparing them to thrive in the dynamic and competitive landscape of the modern SoC Design and Verification workforce.

SDV 507: Project Work

Module Duration: 240 Hours

Objective:

The objective of project work is to demonstrate the candidates' skill and knowledge in solving a real work Engineering problem involving SoC Design or Verification.

Learning Outcomes

After successful completion of this module, the candidate shall be able to:

- Undertake and indecently complete a real world Industry problem involving VLSI Design or Verification using state of the art industry standard tools and practices

Target Audience: B.E./B.Tech./MCA/BCA/NIELIT A Level/M.Sc. (Electronics/CS)

Prerequisite: Completion of modules relevant to the chosen project problem.

Description

The participants can choose projects involving one among the following;

RTL Design, RISC Processor Based SoC Design, Verification, SoC Applications, etc.