**National Institute of Electronics & Information Technology, Aurangabad**
( राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, औरंगाबाद )
**Ministry of Electronics & Information Technology**
**Government of India**

## COURSE PROSPECTUS

**Name of the Group:** VLSI Design

**Name of the Course: Foundation course in VLSI Design**

**Course Code:** 2022/EHW/NIELIT/05319

**Starting Date: -** 14/08/2023 (Tentative)

**Duration:** 4 Weeks – 90 Hours

**Course Coordinator: Mr. Shashank Singh, Scientist B, NIELIT Aurangabad**

**Objective of the Course: -**

1. To provide a broad working knowledge in Digital IC and FPGA design flow.

2. To give a basic understanding of Verilog RTL coding, simulation, synthesis and an ability to read and interpret the existing code.

3. To give an overview about IC fabrication process.

**Outcome of the Course: -**
On successful completion of the course, a person will develop experience on working with the FPGA kit. The person will understand the basics of VLSI with reference to a case study including the reference architecture, functional blocks and various applications with deep insights into the multiple design challenges. The person will develop insights into

• Digital IC and FPGA Design flow.

• Hardware modeling and simulation using Verilog HDL

• Combinational and sequential circuit design, simulation and synthesis.

• Writing test benches and test automation.

• FPGA implementation of complex digital designs.

**Expected Job Roles:-**

VLSI Design Engineer

FPGA Design Engineer

RTL Design Engineer

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## Course Structure:

| Sr. No. | Module Title | Duration (Hours) | |
|---|---|---|---|
| | | Theory | Lab |
| 1 | Introduction to Digital Electronics | 6 | 4 |
| 2 | Basics of Digital VLSI Technology | 8 | 4 |
| 3 | Fabrication Process and Layout Design Rules | 4 | 2 |
| 4 | Digital CMOS Design | 6 | 6 |
| 5 | Hardware Modeling Using Verilog | 10 | 18 |
| 6 | Implementation of Logic gates/circuits in Verilog using Tool (ModelSim or Xilinx) | 6 | 16 |
| **Total** | | **90 Hours (Theory-40, Lab-50)** | |

## Other Contents:

**I.** **Course Fees :** Course fee is Rs 10,000 including GST (*NIL for SC/ST)
II. **Registration Fee:** Rs.1000/- (including all taxes as applicable) (*NIL for SC/ST)
III. **Course Fee Installment Structure:-** Not Applicable for this course
**IV.** **Eligibility:** Diploma/B.E./B.Tech./MSc. in Electronics/Computer Science (All allied branches). (Final Year MSc/Diploma students/3rd and 4th Year B.E./B.Tech can also apply)
**V.** **Number of Seats :40**
VI. **Selection of candidates :** First cum First Served basis.
VII. **Test/Interview (if applicable) :** Not Applicable
**VIII.** **Counselling/Admission :** Starting date of the course
**IX.** **Important Dates (if applicable) :**

| | |
|---|---|
| **Starting date:** | **14/08/2023** (Tentative) |
| **Last date to submit application form:** | **11/08/2023** |
| **Counselling/Admission** | **11/08/2023** |
| **Commencement of class work:** | **14/08/2023** |
| **Payment of Fee** | **11/08/2023** |

X. **Course Timings :** 16:30 Hrs to 18:30 Hrs
**XI.** **Placement :** Support shall be provided
**XII.** **Lab Facilities:**
LIST OF EQUIPMENT (For a batch of 40 students)

| Sr. NO. | Description | Qty |
|---|---|---|
| 1 | Classroom | 2 |
| 2 | Student Chair | 40 |

| | | |
|---|---|---|
| 3 | Student Table | 20 |
| 4 | Smart Interactive Display | 2 |
| 5 | White Board | 2 |
| 6 | Desktop computer with accessories | 40 |
| 7 | Basys 3 Artix-7 FPGA Board | 40 |

**XIII. Registration Details: -**

https://docs.google.com/forms/d/1txAbGMtUdLyDIXRQV7Ta1RlbCYDHZrsNMl-NnjtL39M/edit?pli=1