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National Institute of Electronics & Information Technology (NIELIT) Aurangabad

CEDTI Complex ,Dr Babasaheb Ambedkar Marathwada University Campus, Aurangabad, Maharashtra 431004

Short term Course (NSQF Aligned) In

Certified VLSI Design Engineer

Course Prospectus & Detailed Curriculam

COURSE PROSPECTUS

Name of the Department: *Electronics*

Name of the Course: *Short term course in Certified VLSI Design Engineer (NSQF Aligned)*

Course Code: 2022/EHW/NIELIT/06345

Starting Date: *19 August 2024*

Duration: *480 Hours*

Course Coordinator : Shri. Shashank Kumar Singh**,** 91-9999026637, shashank@nielit.gov.in
Course Co-coordinator : Shri. Ravi Ranjan Kumar , 91-9671501662, raviranjan@nielit.gov.in

Course Preamble:

Complex Very Large Scale Integrated (VLSI) systems are typically constructed on System on Chips (SoCs). Within an SoC, multiple processor cores and essential peripherals are commonly integrated. Designing an SoC necessitates expertise in processor architectures, diverse bus protocols, and related areas. Moreover, verifying an SoC presents significant challenges due to the multitude of complex scenarios involved. Consequently, SoCs are often emulated on Field Programmable Gate Arrays (FPGAs) to facilitate verification, with final chip verification conducted prior to fabrication.

This SoC Design and Verification course is tailored to equip participants with the essential industry skills needed for roles in SoC Design, Verification, and FPGA Emulation projects. It specifically emphasizes industry-standard RISC processor-based SoC design, verification, and FPGA emulation. Key skills such as Verilog HDL Coding for synthesis, FPGA Architecture and programming, and System Verilog-based Verification are comprehensively covered, ensuring participants are well-prepared for employment in the industry. Successful completion of the course will transform participants into professionals who are immediately employable in the field. Furthermore, it provides valuable support to startup industries operating in the SoC Design, Verification, and Emulation domain.

Objective of the Course

- To provide detailed knowledge in semicustom IC design flow, digital logic design, hardware modeling using Verilog HDL, RTL coding, simulation and synthesis.
- To provide in-depth knowledge in IP Core design, FPGA emulation and debugging.
- To provide detailed knowledge in CMOS circuit design and IC layout techniques.
- To give an overview of VLSI Verification techniques and methodologies.
- Entrepreneurship Development.

Moreover, the objectives of this course are aligned to the National Policy on Electronics (NPE) by the Govt of India. Please refer this page: http://meity.gov.in/esdm for more details.

Outcome of the Course:

This course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries like:

(a) VLSI Frontend and backend design
(b) FPGA Emulation/FPGA based embedded system design

For people interested in entrepreneurships this would be an excellent launch pad. In addition, the course also serves as a concrete platform for people involved in application research, consultancy and high-end product development in both industry and academia.

Expected job roles

● VLSI Design Engineer

● FPGA Design Engineer

● Physical Design Engineer

● RTL Design Engineer

Course Structure

Sr. No.	Module Title	Duration (Hours)
1	**Introduction To Digital Electronics**	35
2	**Introduction To VLSI**	35

3	**Verilog HDL**	50
4	**Modeling Techniques**	70
5	**FPGA Architecture and Prototyping**	50
6	**Introduction to the MOS Technology**	50
7	**VLSI Circuit Design Processes**	70
8	**Design Verification UVM, OVM and AVM Methodology**	60
9	**Employability Skills**	30
10	**On Job Training**	30
Total		**480 Hours**

Duration: 480 Hours

Other contents

Course Fees: Rs. 21,600/- + GST and other taxes if any as applicable (* NIL for SC/ST)

Registration fee: An amount of Rs.1000/- (including all taxes as applicable) should be paid at the time of registering for the course . (For SC/ST , Registration fee will be reimbursed after successful completion of the course)

Course Fee Installment Structure: Can be paid in two instalments

Eligibility: B.E./B.Tech./MSc. in Electronics/Computer Science (All allied branches). (Final Year students can also apply)

Number of Seats : *40*

Selection of candidates :

The selection to the course shall be based on the following criteria: Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

Test/Interview: *Not Applicable*

Counselling/Admission: *All candidates will have to be present personally for* ***counseling and admission on 12th August 2024*** *with all the necessary documents (originals and attested copies). Working days are from Monday to Friday. Admission timings are from 9.30 am to 5.00 pm.*

Important Dates:

Starting date:	**19/08/2024 (Tentative)**
Last date to submit application form:	**12/08/2024**
Counselling/Admission	**12/08/2024**
Commencement of class work:	**19/08/2024**
Payment of Fee	**12/08/2024**

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The classes and labs are from 9.30 am to 01:00 pm and 1.30 pm to 5:00 pm Monday to Friday.

Placement:
We have a placement cell, which provides placement assistance to students who qualify our courses.
Also , *The course improves the knowledge and skill of the students as it deals with the latest technologies and tools used in industries. This helps the student in getting a placement by*

i. Campus placement

ii. Placement by companies for whom we send the students bio data and they conduct interviews at their site.

iii. Students themselves attend interview at different companies and the course helps in the interview.

Lab Facilities *: NIELIT Aurangabad is a participating institute under C2S Programme of MeitY along with other elite 100 institutions across the country. The VLSI, FPGA and SoC Design Labs are equipped with Industry standard VLSI Design tools from Synopsys, CADENCE, AMD (Xilinx) and SIEMENS-Mentor.*

Course Contents :

Sr. No.	Module Title
1	**Introduction To Digital Electronics** • Introduction to Number Systems, Logic Gates • Understanding Combinational Logic Circuit Designing -Adder, Subtractor, MUX, DEMUX, Encoder and Decoder etc. • Understanding Sequential Logic Circuit Designing-Latches, Flipflops, Counter, Register etc. • Introduction to Finite state machine (FSM) • Moore's Machine and Mealy's Machine.
2	**Introduction To VLSI** • Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design
3	**Verilog HDL** • Overview of Digital Design with Verilog HDL • Evolution of CAD • Emergence of HDLs, typical HDL-based design flow • Why Verilog HDL, trends in HDLs. • Hierarchical Modeling Concepts • Top-down and bottom-up design methodology • Differences between modules and module instances • Parts of a simulation, design block, stimulus block • Basic Concepts Lexical conventions • Data types, system tasks, compiler directives • Modules and Ports Module definition • Port declaration, connecting ports • Hierarchical name referencing
4	**Modeling Techniques** • Gate-Level Modeling • Modeling using basic Verilog gate primitives, description of and/or and buf/not type

	gates, rise • Fall and tum-off delays, min, max, and typical delays. Dataflow Modeling ● Continuous assignments • Delay specification, expressions, operators, operands, operator types • Behavioural Modeling Structured procedures • Initial and always, blocking and nonblocking statements • Delay control, Event control • Conditional statements, multiway branching loops, sequential and parallel blocks • Tasks and Functions • Differences between tasks and functions • Declaration, invocation • Useful Modeling Techniques • Procedural continuous assignments • Overriding parameters • Conditional compilation and execution • Useful system tasks.
5	**FPGA Architecture and Prototyping** • Introduction to FPGA, Architecture • Internal resource and Design Essentials • FPGA Input/output Blocks (IOBs), Special FPGA functions • Logic Synthesis, FPGA Programming with Verilog basics, Tool Training • Different Voltage Requirement's for FPGA • Different External memory devices architecture • IO Planning, Report analysis for Timing, Area and Power • CPLD, FPGA working, References, Design flow, Design tricks • H/W components on FPGA board and their working • Designing basic FPGA examples (Adder, Subtractor, Counter etc.)
6	**Introduction to the MOS Technology** • Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies • Basic Electrical Properties of MOS and BiCMOS Circuits • IDS - VDS relationships • MOS transistor Threshold Voltage • Figure of merit, Transconductance • Pass transistor • NMOS Inverter, Various pull ups • CMOS Inverter analysis and design • Bi-CMOS Inverters • Fabrication Process Flow • Transmission gates etc • Device sizing, timing parameters • Estimation of layout resistance & capacitance
7	**VLSI Circuit Design Processes**

	• VLSI Design Flow • MOS Layers • Stick Diagrams, Design Rules and Layout • Lambda(λ)-based design rules for wires, contacts and Transistors • Layout Diagrams for NMOS and CMOS Inverters and Gates • Scaling of MOS circuits, Limitations of Scaling. • Introduction to simulation tools • Place and Route Extraction, LVS • Netlist to GDS-II flow • Device Generator Libraries • SPICE Modelling, SPICE Tutorials and Commands • Sources and Passive Components • Inverter Transient
8	**Design Verification UVM, OVM and AVM Methodology** • Introduction UVM, UVM Object • UVM test Bench etc. • Introduction OVM, OVM Reporting • OVM Transaction • OVM Configuration etc. • Need for File Inter Change • GDS2 Stream, Caltech Intermediate Format (CIF) • Library Exchange Format (LEF) • Design Exchange Format (DEF), Standard Delay Format (SDF), DSPF • SPEF, Advance Library Format (ALE), Waves Waveform and Vector Exchange • Specification, Physical Design Exchange Format, Open Access
9	**Employability Skills** • Introduction to Employability Skills • Career Development & Goal Setting • Becoming a Professional in the 21st Century • Basic English Skills • Communication Skills • Financial and Legal Literacy • Entrepreneurship • Diversity & Inclusion • Constitutional values - Citizenship • Essential Digital Skill
10	**On Job Training**