National Institute of Electronics & Information Technology, Aurangabad
(राष्ट्रीयइलेक्ट्रॉनिकीएवंसूचनाप्रौद्योगिकीसंस्थान,औरंगाबाद)
Ministry of Electronics & Information Technology
Government of India

COURSE PROSPECTUS

Name of the Group: VLSI Design

Name of the Course : Certified VLSI Design Engineer

Course Code:2022/EHW/NIELIT/06345

Starting Date:14/08/2023 (Tentative)

Duration:480 Hours

Course Coordinator : Mr. Shashank Singh, Scientist B, NIELIT Aurangabad

Course Objectives:

- To provide detailed knowledge in semicustom IC design flow, digital logic design, hardware modeling using Verilog HDL, RTL coding, simulation and synthesis.
- To provide in-depth knowledge in IP Core design, FPGA emulation and debugging.
- To provide detailed knowledge in CMOS circuit design and IC layout techniques.
- To give an overview of VLSI Verification techniques and methodologies.
- Entrepreneurship Development.

Moreover, the objectives of this course are aligned to the National Policy on Electronics (NPE) by the Govt of India. Please refer this page: http://meity.gov.in/esdm for more details.

Outcome of the Course: -
This course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries like:

(a) VLSI Frontend and backend design
(b) FPGA Emulation/FPGA based embedded system design

For people interested in entrepreneurships this would be an excellent launch pad. In addition, the course also serves as a concrete platform for people involved in application research, consultancy and high-end product development in both industry and academia.

Expected Job Roles:

● VLSI Design Engineer

● FPGA Design Engineer

● Physical Design Engineer

● RTL Design Engineer

Course Structure:

Sr. No.	Module Title	Duration (Hours)
1	**Introduction To Digital Electronics** • Introduction to Number Systems, Logic Gates • Understanding Combinational Logic Circuit Designing -Adder, Subtractor, MUX, DEMUX, Encoder and Decoder etc. • Understanding Sequential Logic Circuit Designing- Latches, Flipflops, Counter, Register etc. • Introduction to Finite state machine (FSM) • Moore's Machine and Mealy's Machine.	35
2	**Introduction To VLSI** • Need, Scope, Use and History of VLSI • Introduction to Chip Design Process • Description of Hardware Description Languages • Applications of VLSI • VLSI Design Flow • Moore's Laws • VLSI Design Flow and Y-Chart • Front-Back End VLSI Design	35
3	**Verilog HDL** • Overview of Digital Design with Verilog HDL • Evolution of CAD • Emergence of HDLs, typical HDL-based design flow • Why Verilog HDL, trends in HDLs. • Hierarchical Modeling Concepts • Top-down and bottom-up design methodology • Differences between modules and module instances • Parts of a simulation, design block, stimulus block • Basic Concepts Lexical conventions • Data types, system tasks, compiler directives • Modules and Ports Module definition • Port declaration, connecting ports • Hierarchical name referencing	50
4	**Modeling Techniques** • Gate-Level Modeling • Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise	70

	• Fall and tum-off delays, min, max, and typical delays. Dataflow Modeling ● Continuous assignments • Delay specification, expressions, operators, operands, operator types • Behavioural Modeling Structured procedures • Initial and always, blocking and nonblocking statements • Delay control, Event control • Conditional statements, multiway branching loops, sequential and parallel blocks • Tasks and Functions • Differences between tasks and functions • Declaration, invocation • Useful Modeling Techniques • Procedural continuous assignments • Overriding parameters • Conditional compilation and execution • Useful system tasks.	
5	**FPGA Architecture and Prototyping** • Introduction to FPGA, Architecture • Internal resource and Design Essentials • FPGA Input/output Blocks (IOBs), Special FPGA functions • Logic Synthesis, FPGA Programming with Verilog basics, Tool Training • Different Voltage Requirement's for FPGA • Different External memory devices architecture • IO Planning, Report analysis for Timing, Area and Power • CPLD, FPGA working, References, Design flow, Design tricks • H/W components on FPGA board and their working • Designing basic FPGA examples (Adder, Subtractor, Counter etc.)	50
6	**Introduction to the MOS Technology** • Introduction to IC technology MOS, PMOS, NMOS, CMOS &BiCMOS Technologies • Basic Electrical Properties of MOS and BiCMOS Circuits • IDS - VDS relationships • MOS transistor Threshold Voltage • Figure of merit, Transconductance • Pass transistor	50

	• NMOS Inverter, Various pull ups • CMOS Inverter analysis and design • Bi-CMOS Inverters • Fabrication Process Flow • Transmission gates etc • Device sizing, timing parameters • Estimation of layout resistance & capacitance	
7	**VLSI Circuit Design Processes** • VLSI Design Flow • MOS Layers • Stick Diagrams, Design Rules and Layout • Lambda(λ)-based design rules for wires, contacts and Transistors • Layout Diagrams for NMOS and CMOS Inverters and Gates • Scaling of MOS circuits, Limitations of Scaling. • Introduction to simulation tools • Place and Route Extraction, LVS • Netlist to GDS-II flow • Device Generator Libraries • SPICE Modelling, SPICE Tutorials and Commands • Sources and Passive Components • Inverter Transient	70
8	**Design Verification UVM, OVM and AVM Methodology** • Introduction UVM, UVM Object • UVM test Bench etc. • Introduction OVM, OVM Reporting • OVM Transaction • OVM Configuration etc. • Need for File Inter Change • GDS2 Stream, Caltech Intermediate Format (CIF) • Library Exchange Format (LEF) • Design Exchange Format (DEF), Standard Delay Format (SDF), DSPF • SPEF, Advance Library Format (ALE), Waves Waveform and Vector Exchange • Specification, Physical Design Exchange Format, Open Access	60
9	**Employability Skills** • Introduction to Employability Skills • Career Development & Goal Setting • Becoming a Professional in the 21st Century	30

	• Basic English Skills • Communication Skills • Financial and Legal Literacy • Entrepreneurship • Diversity & Inclusion • Constitutional values - Citizenship • Essential Digital Skill	
10	**On Job Training**	30
Total		**480 Hours**

Other Contents:

I. **Course Fees :**Course fee is Rs 40,000 + GST (* Nil for SC/ST)
II. **Registration Fee :** Rs.1000/- (including all taxes as applicable) (*NIL for SC/ST)
III. **Course Fee Installment Structure:-** Can be paid in two instalments
IV. **Eligibility:** B.E./B.Tech./MSc. in Electronics/Computer Science (All allied branches). (Final Year students can also apply)
V. **Number of Seats :30**
VI. **Selection of candidates: The** candidates passed in the qualifying examination will be based on their marks obtained, subject to eligibility and availability of seats.
VII. **Test/Interview (if applicable) :** Not Applicable
VIII. **Counselling/Admission :** Starting date of the course
IX. **Important Dates (if applicable) :**

Starting date:	**14/08/2023 (Tentative)**
Last date to submit application form:	**11/08/2023**
Counselling/Admission	**11/08/2023**
Commencement of class work:	**14/08/2023**
Payment of Fee	**11/08/2023**

X. **Course Timings :**16:30 Hrs to 19:30 Hrs in week days.
: 9.30 Hrs to 12.30 Hrs in week end days.
XI. **Placement :**Support shall be provided
XII. **Lab Facilities:**
LIST OF EQUIPMENT (For a batch of 30 students)

Sr. NO.	Description	Qty
1	Classroom	2
2	Student Chair	30
3	Student Table	15

4	Smart Interactive Display	2
5	White Board	2
6	Desktop computer with accessories	30
7	Basys 3 Artix-7 FPGA Board	30

XIII. Registration Details: -

https://docs.google.com/forms/d/1txAbGMtUdLyDIXRQV7Ta1RlbCYDHZrsNMl-NnjtL39M/edit?pli=1