This course is intended to impart training in designing and verifying reusable Intellectual Property (IP) Cores for VLSI. Emphasis of the teaching curriculum is on design & Verification methodologies and on its practical applications. The course contents have been designed keeping in view the emerging trends in needs for skilled manpower.

**Eligibility**

B.E/B.Tech/MCA/M.Sc.(Comp.Sc.) (pursuing also) with basic knowledge of statistics, database and any programming language.

**Course Outline**

- Overview of VLSI, Verilog and Digital Design.
- Hierarchical Modelling
- Modules and Ports definition
- Gate Level Modelling
- Data Flow modelling
- Behavioural Modelling
- Structural Modelling

**Course Objective**

Candidate must have ModelSim software installed and latest computer/laptop with preferably 4 GB RAM or higher.

**Course Duration**

04 weeks/06 weeks* - Online Mode

Note:*6 weeks Programme includes two weeks project. No additional fee will be charged for Project.

**Prerequisites for Online Class**

Candidate may apply online at following link: [http://nielit.gov.in/haridwar/content/online-courses](http://nielit.gov.in/haridwar/content/online-courses). Fee is to be submitted to the following account and details to be submitted in online registration form.

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For further information/clarification, please contact on 9368499990.

Contact Details: NIELIT Haridwar, 2nd Floor, Government Polytechnic Building, Plot No-6C, Sector-11, Near Pentagon Mall, SIDCUL, Haridwar, Uttarakhand – 249403, Phone:- 01334-235617, 235054, 9368349990 E-Mail: haridwar@nielit.gov.in

For Registration

CLICK HERE