

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

### Preamble:

As per the IESA's data, there are over 250 companies in India, working in the areas of chip design, embedded systems and board design representing all major industry verticals including Telecommunications, Networking, Consumer Electronics, Industrial, Healthcare, Automotive and others and there is a huge demand for high quality trained manpower VLSI domain. This course has been designed to bridge this skill gap and provides participants with strong foundation, much needed for;

- Hardware Modelling & Test benching
- Designing Intellectual Property (IP) cores for VLSI
- Hardware Prototyping using Field Programmable Gate Arrays (FPGAs) of high logic density
- RTL Verification and Digital IC (ASIC) Design
- Microcontroller based System Design & Prototyping
- PCB Designing etc

### Objective:

The PG Diploma in VLSI & Embedded Hardware Design is intended to impart training in designing complex embedded systems using reusable Intellectual Property (IP) Cores as building blocks and employing hierarchical design methods. Emphasis of the teaching curriculum is on design methodology and practical applications. The course contents have been designed keeping in view the emerging trends in needs for skilled manpower.

### Expected Job Roles:

- RTL Design Engineer
- RTL Verification Engineer
- FPGA design Engineer
- Board Design Engineer
- Physical Design Engineer

### Duration:

**720 Hours - (Theory: 140 hrs + Practical: 370 hrs+ Project: 210 Hours)**

**This course shall be offered as full time intensive course.**

### Course Outline:

Sl. No	Module Title	Duration (Hours)			Credits	
		Theory	Lab	Total	Theory (hrs/15)	Lab (hrs/30)
1	Advanced Digital Design	25	05	30	2	0

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

2	Verilog HDL: Language and Coding for Synthesis	20	70	90	1	2
3	RTL Verification	30	120	150	2	4
4	FPGA Design Methodology and Prototyping	15	45	60	1	2
5	CMOS Logic & Physical Design	25	65	90	2	2
6	Embedded Controller Based Product Design	25	65	90	2	2
7	Project Work	0	210	210	0	7
<b>Total Duration/Credits</b>		<b>140</b>	<b>580</b>	<b>720</b>	<b>29</b>	

### Prerequisites:

Knowledge of Basic Electronics

### Eligibility:

BE/B.Tech (ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) / M.Sc (Electronics/CS). Students undergoing BTech/ MSc are also eligible, however they will be issued course certificate only on production of their degree certificate.

### Detailed Syllabus and Learning Outcome:

S. No	Module Title	Topics	Duration (Hours)		Learning Outcome
			Theory	Lab	
1	<b>Advanced Digital Design</b>	<ul style="list-style-type: none"> <li>Combinational Circuit Design</li> <li>Sequential Circuit Design</li> <li>Design of controller and Data path units</li> <li>State Machines</li> <li>Design Examples &amp; Case Studies</li> </ul>	25	05	After successful completion of the module, the students shall be able to: <ul style="list-style-type: none"> <li>Design Control and Data path Units</li> </ul>
2	<b>Verilog HDL: Language and Coding for Synthesis</b>	<ul style="list-style-type: none"> <li>Introduction to Verilog HDL &amp; Hierarchical Modeling Concepts</li> <li>Lexical Conventions &amp; Data Types</li> <li>System Tasks &amp; Compiler Directives</li> <li>Modules, Ports and Module</li> </ul>	20	70	After successful completion of the module, the students shall be able to: <ul style="list-style-type: none"> <li>Author Design IPs for VLSI using Verilog HDL</li> <li>Develop Test benches</li> </ul>

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

		<p>Instantiation Methods</p> <ul style="list-style-type: none"> <li>• Gate Level Modeling</li> <li>• Dataflow Modeling</li> <li>• Behavioral Modeling</li> <li>• RTL Design and Logic Synthesis and Synthesis issues</li> <li>• Design Verification using Test benches</li> <li>• Mini-project and Case Studies</li> </ul>			using Verilog HDL
3.	<b>RTL Verification</b>	<ul style="list-style-type: none"> <li>• Functional Verification – Concepts, Simulators, Coverage and Metrics</li> <li>• Introduction to Verification Methodologies</li> <li>• Testing strategy – Directed and random Testing</li> <li>• Test Cases Vs Test Benches</li> <li>• Verification Components (Drivers, Checkers, Monitors, Scoreboards etc.)</li> <li>• Case study of a Verification IP</li> <li>• System Verilog</li> <li>• Object oriented programming for ASIC Design &amp; Verification</li> <li>• Functional Verification</li> <li>• Assertion based verification</li> <li>• Coverage Driven Verification</li> <li>• Coverage Analysis</li> <li>• PLI and DPI Basics</li> <li>• Universal Verification Methodology</li> <li>• UVM Components and practices</li> <li>• Verification IP Design</li> </ul>	30	120	<p>After successful completion of the module, the students shall be able to:</p> <ul style="list-style-type: none"> <li>• Author Verification IPs</li> <li>• Perform Coverage Driven Verification</li> <li>• Perform assertion based verification</li> <li>• Perform functional Verification</li> <li>• Perform UVM based RTL verification</li> </ul>
4.	<b>FPGA Design Methodology and Prototyping</b>	<ul style="list-style-type: none"> <li>• Introduction to Programmable Logic and FPGAs</li> <li>• Popular CPLD &amp; FPGA Families</li> <li>• Architecture of popular Xilinx and Altera FPGAs</li> </ul>	15	45	<p>After successful completion of this module, students should be able to:</p> <ul style="list-style-type: none"> <li>• FPGA based prototyping</li> </ul>

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

		<ul style="list-style-type: none"> <li>• FPGA Design Flow Altera Quartus II</li> <li>• FPGA Design Flow Xilinx ISE</li> <li>• Implementation Details</li> <li>• Advanced FPGA Design tips</li> <li>• Logic Synthesis for FPGA</li> <li>• Static Timing Analysis</li> <li>• Design problems using Xilinx Platforms</li> <li>• Design problems using Altera Platforms</li> <li>• Case Studies on FPGA Based implementations</li> <li>• IP Reuse Methodology</li> <li>• Soft IP vs Hard IP</li> <li>• IP Design Process &amp; System Integration with reusable IP</li> </ul>			<ul style="list-style-type: none"> <li>• Design Interfacing</li> <li>• Generate reusable IP s</li> </ul>
5.	<b>CMOS Logic &amp; Physical Design</b>	<ul style="list-style-type: none"> <li>• MOS Fundamentals</li> <li>• MOS Switches &amp; Designs</li> <li>• Transmission Gates</li> <li>• Inverter – DC</li> <li>• AC Characteristics</li> <li>• Combinational and Sequential Logic</li> <li>• Introduction to Layout Tools</li> <li>• Introduction to IC Layout</li> <li>• IC Layout Design tools</li> <li>• RTL to GDS II</li> <li>• Introduction to Physical Verification (DRC, LVS, SoftCheck, Antenna Effect and DFM)</li> <li>• Layout design rules &amp; techniques</li> <li>• Circuit examples</li> </ul>	25	65	<p>After successful completion of the module, the students shall be able</p> <ul style="list-style-type: none"> <li>• Perform CMOS Logic Design</li> <li>• Perform Physical Design for VLSI</li> <li>• Perform GDS II Streaming needed for chip fabrication</li> </ul>
6.	<b>Embedded Controller Based Product Design</b>	<ul style="list-style-type: none"> <li>• Quality principles and tools</li> <li>• Product Development Process</li> <li>• System level design using hardware and software</li> </ul>	25	65	<p>After successful completion of the module, the students shall be able</p> <ul style="list-style-type: none"> <li>• Code embedded software</li> </ul>

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

		<ul style="list-style-type: none"> <li>• Hardware and software integration issues and testing</li> <li>• Hardware and software co-verification</li> <li>• Component cost and costing in product design</li> <li>• Case studies of real life designs</li> <li>• Industrial Design</li> <li>• Project Management (PERT/CPM) MS Project</li> <li>• Interconnection design &amp; EDA tools</li> <li>• Thermal Design</li> <li>• Documentation</li> <li>• Team work and communication</li> <li>• Embedded Product design Syndicate</li> <li>• EMI/EMC</li> <li>• Case study of Microcontroller based Design</li> <li>• Project Design phase</li> <li>• Hardware design and construction</li> <li>• Software design and development</li> <li>• Integration and debugging of hardware and software</li> <li>• Final testing</li> <li>• ORCAD Schematic and PCB Layout</li> <li>• Mini Project</li> </ul>			<ul style="list-style-type: none"> <li>• Deal with hardware and software integration issues</li> <li>• Perform Design , test and validation of PCBs</li> </ul>
7.	<b>Project Work</b>	<p>The project should involve any one or combination of the below</p> <p>Design IP Verification IP Physical Design for VLSI Microcontroller based System /SoC</p>	0	210	After successful completion of the module, the participants should be able to identify problem statement, perform through literature survey , design, develop and validate /prototype IPs for VLSI /Embedded Systems

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

<b>Total Hours = 720</b>	140	580	
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### Examination & Certification:

NIELIT's NSQF Examination pattern will be followed for Examination & Certification.

Sl No	Examination Pattern	Modules Covered	Duration in Minutes	Maximum Marks
1	Theory Paper – 1	1,4,5	90	100
2	Theory Paper – 2	3	90	100
3	Theory Paper – 3	6	90	100
4	Practical -1	2 &4	180	90
5	Practical -2	6	180	90
6	Internal Assessment	Based on all modules	Continuous assessment	60
7	Project/Presentation /Assignment	Based on all modules	Continuous assessment	60
8	Major Project/Dissertation	Work chosen by candidate in consultation with supervisor	Continuous assessment	100
<b>Total</b>				<b>700</b>

Note:

1. Pass percentage would be 50% marks in each component, with aggregate pass percentage of 50% and above.
2. Grading will be as under:

Grade	S	A	B	C	D
<b>Marks Range (in %)</b>	$\geq 85\%$	$\geq 75\% - < 85\%$	$\geq 65\% - < 75\%$	$\geq 55\% - < 65\%$	$\geq 50\% - < 55\%$

3. Theory examination would be conducted online and the paper comprise of MCQ and each question will carry 1 marks.
4. Practical examination/Internal Assessment/ Project/Presentation/Assignment would be evaluated internally.

## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

5. Major Project/Dissertation would be evaluated preferably by External / Subject Expert including NIELIT Officials.
6. Candidate may apply for re-examination within the validity of registration.
7. The examinations would be conducted in English Language only.

### Recommended hardware/software tools:

#### HARDWARE Tools:

- Xilinx FPGA Development Boards (Virtex 6, Spartan 6, Spartan 3, Spartan 2 etc.)
- Altera Development Boards (Stratix II, Cyclone II, III, IV, V etc)
- Logical Analyzer, CROs, Power Supplies, Testing Equipments
- SMD Soldering Station

#### SOFTWARE Tools:

- Mentor Graphics® Design Suite
- Cadence® /Synopsys® Tool Suite for ASIC Design & Verification
- MATLAB™
- Xilinx® FPGA Design suite
- Altera FPGA Design suite
- ARM Keil®
- PCB Design suite ( OrCAD® /Padslogic®)

### Faculty & Support / Lab Instructor:

1. Two faculties with M.E/M.Tech ( ECE/EEE/ CSE) OR PGD (VLSI/Embedded Systems) OR B.E/B.Tech (ECE/EEE/ CSE) with good knowledge and Experience in VLSI & Embedded Hardware Design.
2. One **Support / Lab Instructor** with at least Diploma in (ECE/EEE/ CSE) with good knowledge and Experience in VLSI & Embedded Hardware Design.

### References:

1. Digital Design Principles and Practices by John F Wakerly
2. Digital Design by Morris Mano and Michael Ciletti
3. Basic VLSI Design by Douglas A. Pucknell.
4. Verilog HDL: A Guide to Digital Design and Synthesis, by Samir Palnitkar.
5. Digital Design: An Embedded Systems Approach Using Verilog, by Peter Ashenden.
6. Verilog HDL Design Examples by Joseph Cavanagh
7. Verilog HDL Synthesis – A practical primer by Jayaram Bhasker
8. Verilog Digital System Design by Z. Navabi
9. IEEE Standard 1364-2005 LRM for Verilog Hardware Description Language

10. IEEE Standard 1800 LRM for System Verilog
11. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, by Chris Spear.
12. System Verilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, by Stuart Sutherland, Simon Davidmann & Peter Flake.
13. Universal Verification Methodology (UVM) User's Guide by Accellera.
14. Writing Testbenches: Functional Verification of HDL Models, by Janick Bergeron.
15. CMOS Logic Circuit Design by John P. Uyemura.
16. CMOS VLSI Design by Weste and Harris
17. FPGA Prototyping by Verilog Examples by Pong Chu
18. FPGA Based System Design by Wayne Wolf
19. Advanced FPGA Design BY Steve Kilts
20. Introduction to VLSI Circuits and Systems, by John P. Uyemura.
21. Digital Integrated Circuits: A design perspective, by Jan M. Rabaey & Anantha Chandrakasan.
22. Microelectronics Circuits by Sedra & Smith.
23. CMOS Digital Integrated Circuits, by Sung-Mo Kang & Yusuf Leblebici.
24. Application Specific Integrated Circuits by Michael John Sebastian Smith
25. Cadence Design Environment Guide.
26. Getting Started with UVM: A Beginner's Guide, by Vanessa R. Cooper.
27. Xilinx FPGA User Guide.
28. Altera FPGA User Guide.
29. Let us C by Yashwant Kanetkar.
30. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
31. Art of C Programming, JONES, ROBIN, STEWART, IAN
32. C Programming for Embedded systems, Zurell, Kirk
33. STM32 datasheets, reference manuals & Application notes.
34. Product Design & Development - Karl T Ulrich & Steven D. Eppinger; Mc GrawHill
35. Web:- Data Sheets, Application Notes, Technical Reports and Reference Designs from
  - a. <https://www.altera.com>
  - b. <https://www.xilinx.com>
  - c. <https://www.microchip.com>
  - d. <https://www.intel.com>
  - e. <https://www.amd.com>
  - f. <https://www.arm.com>
  - g. <https://www.cypress.com>
  - h. <https://www.microsemi.com>
  - i. <https://www.opencores.org>
  - j. <https://www.ti.com>



## PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI Design Engineer)

k. <https://design-reuse.com>

<b>Course Name</b>	PG Diploma in VLSI & Embedded Hardware Design (Certified VLSI & Embedded Engineer)	<b>Vertical</b>	VLSI & Embedded Systems
<b>Course Code</b>		<b>Rev No</b>	R4
<b>Prepared By</b>	NANDAKUMAR.R	<b>Aligned NSQF Level</b>	8
<b>NIELIT Centre</b>	Calicut	<b>Last Revised on</b>	03.06.2019



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