**A4-R4: COMPUTER SYSTEM ARCHITECTURE**

**अवधि: 03 घंटे**
**DURATION: 03 Hours**

**अधिकतम अंक: 100**
**MAXIMUM MARKS: 100**

<table>
<thead>
<tr>
<th>नाममाण्डल का नाम:</th>
<th>Name of Candidate: ____________________________</th>
</tr>
</thead>
<tbody>
<tr>
<td>रोल नं.:</td>
<td>Roll No.: ____________________________</td>
</tr>
<tr>
<td>उत्तर-पुस्तिका सं:</td>
<td>Answer Sheet No.: ____________________________</td>
</tr>
<tr>
<td>ओएमआर शीट सं:</td>
<td>OMR Sheet No.: ____________________________</td>
</tr>
</tbody>
</table>

**परीक्षार्थी के हस्ताक्षर:****

**Signature of candidate: ____________________________**

**परीक्षार्थी के लिए निर्देश:****

<table>
<thead>
<tr>
<th>कृपया प्रश्न-पुस्तिका, ओएमआर शीट एवं उत्तर-पुस्तिका मे दिये गए निर्देश को ध्यान पूर्वक पढ़ें।</th>
</tr>
</thead>
<tbody>
<tr>
<td>प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी के अंग्रेजी भाषा मे ही उत्तर दें सकते हैं।</td>
</tr>
<tr>
<td>इस मॉड्यूल/पेपर के दो भाग हैं। भाग एक मे यह प्रश्न और भाग दो में पूर्व प्रश्न है।</td>
</tr>
<tr>
<td>भाग एक &quot;वैकल्पिक&quot; प्रश्न का है जिसके कुल अंक 40 है तथा भाग दो, &quot;व्यक्तिपर्व&quot; प्रश्न है और इसके कुल अंक 60 है।</td>
</tr>
<tr>
<td>भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई ओएमआर उत्तर-पुस्तिका पर, उसमे दिये गए अनुदेशों के अनुसार ही दिये जाने चाहिए। भाग दो की उत्तर-पुस्तिका मे भाग एक के उत्तर नहीं दिये जाने चाहिए।</td>
</tr>
<tr>
<td>भाग एक के लिए अधिकतम समय तीन एक घण्टा निर्धारित की गई है। भाग दो की उत्तर-पुस्तिका, भाग एक की उत्तर-पुस्तिका जगह करने के प्रवास दी जानी गई। तथापि, निर्धारित एक घण्टे से पहले भाग एक पूरा करने वाले परीक्षार्थी भाग एक की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरन्त बाद, भाग दो की उत्तर-पुस्तिका से संबंधित है।</td>
</tr>
<tr>
<td>भाग एक के उत्तरों को ओएमआर शीट पर मार्क किये जाते हैं। वहां परीक्षार्थी एक घण्टे के भीतर उत्तर प्रदान करने वाले परीक्षार्थी पूरे जवाब दे सकते हैं।</td>
</tr>
</tbody>
</table>

**Instructions for Candidate:**

<table>
<thead>
<tr>
<th>Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Question Paper is in English language. Candidate can answer in English language only.</td>
</tr>
<tr>
<td>There are TWO PARTS in this Module/Paper. PART ONE contains FOUR questions and PART TWO contains FIVE questions.</td>
</tr>
<tr>
<td>PART ONE is Objective type and carries 40 Marks. PART TWO is subjective type and carries 60 Marks.</td>
</tr>
<tr>
<td>PART ONE is to be answered in the OMR ANSWER SHEET only, supplied with the question paper, as per the instructions contained therein. PART ONE is NOT to be answered in the answer book for PART TWO.</td>
</tr>
<tr>
<td>Maximum time allotted for PART ONE is ONE HOUR. Answer book for PART TWO will be supplied at the table when the answer sheet for PART ONE is returned. However, candidates who complete PART ONE earlier than one hour, can collect the answer book for PART TWO immediately after handing over the answer sheet for PART ONE.</td>
</tr>
<tr>
<td>Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his Answer sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.</td>
</tr>
</tbody>
</table>

**जब तक आपसे कहा न जाए तब तक प्रश्न-पुस्तिका न खोलें।**

**DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.**
PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “OMR” answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 Von Neumann architecture of computer is mainly characterized by ______
A) Separate storage and signal path ways for their instructions and data
B) Stored-program concept emphasizing storing of data as well as the instructions to manipulate that data, in the same way
C) Swiftly execution of program
D) None of the above

1.2 The number of MINITERMS is a truth table of n variables
A) \( n^2 \)
B) \( 2^n \)
C) \( 2^n \)
D) \( n! \)

1.3 In memory hierarchy, which one of the followings is the fastest memory?
A) Magnetic Disk
B) RAM
C) Cache
D) ROM

1.4 Which of the following is not associated with DMA?
A) Bus Request
B) Burst Transfer
C) Programmed I/O
D) Cycle Stealing

1.5 Locality of reference refers to
A) Scope of local variables in functions
B) The area in the memory where the address of instruction is stored
C) The fact that reference to memory at any given interval of time, during the program execution tends to confine with few localized areas in the memory
D) None of the above

1.6 _______ decodes operation code of instruction.
A) Multiplexer
B) Decoder
C) Encoder
D) Demultiplexer

1.7 _______ is a binary coded hexadecimal equivalent of \((01100110)_2\).
A) 66
B) 77
C) 44
D) 99

1.8 CPU processes instruction which resides in _______.
A) Program Counter
B) Instruction Register
C) Address Register
D) Index Register

1.9 _______ memory gives illusion of large memory.
A) Associate
B) Set-Associate
C) Segmented
D) Virtual

1.10 In _______ mode, the operands are specified implicitly in the definition of the instruction.
A) Implied
B) Implicit
C) Direct
D) Indexing

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the “OMR” answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 A combination circuit that performs the arithmetic addition of two bits is called half-adder.

2.2 An overflow condition can be detected by observing carry into sign bit position and carry out of sign bit position.

2.3 A logical shift left operation divides signed binary number by 2.

2.4 Booth’s algorithm is used to add two negative numbers.

2.5 Shift instruction can be categorized under data manipulation instruction.

2.6 Pseudo instructions are assembler directive.

2.7 In memory hierarchy, cost of saving of one bit of information is minimum in cache memory.

2.8 A register is a group of flip-flops with each flip-flop capable of storing one bit of information.

2.9 A register capable of shifting its binary information in one or more direction is called demultiplexer.

2.10 \((74.24)_{10}\) is equivalent to \((1111011.11011)_{2}\).
3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “OMR” answer sheet supplied with the question paper, following instructions therein. (1x10)

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 A digital circuit which forms arithmetic sum of two bits &amp; a previous carry</td>
<td>A. Cache</td>
</tr>
<tr>
<td>3.2 Memory unit access by content</td>
<td>B. Post-Fix</td>
</tr>
<tr>
<td>3.3 Second part of an instruction code containing operand</td>
<td>C. Vectored Interrupt</td>
</tr>
<tr>
<td>3.4 Converting expression to evaluate arithmetic expression in stock operations</td>
<td>D. 2 stable states</td>
</tr>
<tr>
<td>3.5 In interrupt Initiated I/O, branch address is arranged to a fixed local in memory</td>
<td>E. Immediate instruction</td>
</tr>
<tr>
<td>3.6 Flip-Flop loss</td>
<td>F. No. of tasks completed per unit time</td>
</tr>
<tr>
<td>3.7 Throughput is defined as</td>
<td>G. FULL Address</td>
</tr>
<tr>
<td>3.8 Shift Register</td>
<td>H. Page replacement</td>
</tr>
<tr>
<td>3.9 LRU</td>
<td>I. Associative memory</td>
</tr>
<tr>
<td>3.10 One I/P signal to the gate &amp; one O/P signal from the gate</td>
<td>J. NOT Gate</td>
</tr>
<tr>
<td></td>
<td>K. Direct instruction</td>
</tr>
<tr>
<td></td>
<td>L. Infixed</td>
</tr>
<tr>
<td></td>
<td>M. Can shift its stored data by one bit postern at each clock period</td>
</tr>
</tbody>
</table>

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Choose the most appropriate option, enter your choice in the “OMR” answer sheet supplied with the question paper, following instructions therein. (1x10)

| A. -127 | B. linker | C. AND |
| D. Flip-flops | E. Multiprogramming | F. Compiler |
| G. Program Counter | H. Bootstrap | I. -128 |
| J. DMA | K. ADDER | L. Mantissa |
| M. Multiplexer |

4.1 A _______ is a program which is started first when computer is powered ON.
4.2 A high level language is converted into machine level language by _______.
4.3 Floating point representation contains _______ and exponent.
4.4 The storage element employed in a clocked sequential circuit are called _______.
4.5 _______ is a combinational circuit that receives binary information from one of the 2^n input lines and directs it to a single output line.
4.6 In _______, several programs reside in main memory.
4.7 _______ stores the address of next instruction to be executed.
4.8 _______ transfers data from I/O devices to main memory without involvement of CPU.
4.9 In half adder, CARRY can be obtained by using _______ gate.
4.10 The smallest negative number that can be represented in 8-bit two's complement form is _______.
PART TWO
(Answer any FOUR questions)

5. a) Draw and explain logic circuit diagram of Encoder and Decoder.
   b) What are the differences between circular shift and arithmetic shift?
   c) What is instruction pipeline? What are the problems associated with Instruction pipeline?

6. a) During execution of instruction, the way the operands are chosen depends on addressing mode of instruction. Which are the modes of addressing? Specify effective address of operand for each addressing mode.
   b) Write a short Note on DMA.

7. a) Perform following arithmetic operation using 2’s complement integers.
   i) 35+ (-10)
   ii) 20 - (-4)
   b) Write an assembly language program to multiply two positive numbers. (Numbers are 13_{10}, 10_{10}).
   c) Which are the registers used in basic computer organization? Write function of each register.

8. a) How are Instruction Register (IR) & Control Unit (CU) connected to decode instruction?
   b) Draw and explain flow chart for Booth Multiplication Algorithm.

9. a) What is disadvantage of strobe method? Explain in brief source-initiated data transfer procedure using handshaking along with its block diagram and timing diagram?
   b) Why do computers use addressing mode techniques? Explain Immediate, indexed, Relative & Base register addressing modes.
   c) How does microprocessor handles I/O interrupts. Draw Flow chart.

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