No. of Printed Pages : **2**

Sl. No.

C0-R4.B4 : COMPUTER SYSTEM ARCHITECTURE

NOTE :

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours | Total Marks: 100

1. (a) Represent the following conditional control statement by two register transfer statements with control function.

if (P = 1) then (R1 ← R2) else if (Q = 1) then (R1← R3)

(b) What are the four main functions of a computer?

(c) Addresses in an 8 bit machine are 16 bit wide. How many memory accesses are necessary to execute an instruction ? Assume that the machine is memory-memory and operands are specified using absolute addresses.

(d) What is pipelining ?

(e) What are the basic rules of the assembly language of the basic computer ?

(f) Differentiate between RAM and ROM.

(g) Explain the term: Programmed I/O. **(7×4)**

2. (a) Draw and explain Four-segment CPU Pipeline.

(b) Define the following :

(i) micro-operation ;

(ii) microinstruction ;

(iii) micro-program ;

(iv) microcode. **(10+8)**

3. (a) Explain Flynn's classification of computer architecture.

(b) Perform addition and subtraction using signed 2's complement system.

(i) $(-29)_{10} + (+49)_{10}$

(ii) $(1001)_2 - (01111)_2$

(c) Explain with an example, how is effective address calculated in different types of addressing modes. **(10+4+4)**

4. (a) Compare RISC and CISC architecture.

(b) Use the booth algorithm to multiply -119 (multiplicand) by +11(multiplier), where each number is represented using 6-bit signed numbers.

(c) What is direct memory access (DMA) ? Why are the read and write control lines in a DMA controller bi-directional ? **(6+6+6)**

5. (a) What is Register Transfer Language ? Explain commonly used registers in RTC.

(b) Show the content of the stack while implementing the statement : a = a + b + a * c (on zero-address machines). **(8+10)**

6. (a) What do you mean by asynchronous data transfer ? Explain strobe control in detail.

(b) What is an Interrupt Cycle ? Draw and explain flow chart of it. **(10+8)**

7. (a) Explain hazards to the instruction pipeline with their solution.

(b) Describe following terms :

(i) Bus Interface Unit

(ii) Cache Memory **(9+9)**

- o O o -