**Certificate Course in**

**VLSI System Design using FPGA**

**1. Objective:**

This course aims to providing detailed knowledge in VLSI design process starting from digital design, hardware descriptive languages, RTL Design, synthesis & simulation, verification, FPGA programming & implementation. The course is intended to give the student an understanding of the fundamental system level electronic issues involved in the design of digital deep submicron CMOS VLSI systems and a mastery of the basic techniques and methods used to deal with VLSI RTL Design and Verification and implementation upon FPGA’s. In this process the learners are well trained to understand the entire logic design process and are well equipped to take on the challenges posed by the even demanding chip design industry.

**2. Learning Outcome:**

After the end of the course the student will be able to complete a significant VLSI design project having a set of objective criteria and design constraints.

**3. Duration of the course:** 300 hrs.

**4. Minimum eligibility criteria to enroll in this course:**

1. Pursuing or Passed students of Diploma in Electronics/ Electronics & Communication/Electrical/Electrical & Electronics/ Instrumentation/ Biomedical /Computer Science/Information Technology.
2. Pursuing or Passed students of B.Sc./B.Tech/M.Sc./M.Tech/ Polytechnic/ITI in Electronics & Communication / Instrumentation/Computer Science/Information Technology.

**5. Syllabus Outline:**

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| **Sr. No.** | **Topics** | **No. of Hours** |
| **1.** | Introduction to VLSI | 30 |
| **2.** | Advanced Digital Design | 30 |
| **3.** | VHDL: Language and Coding for Synthesis | 30 |
| **4.** | Verilog HDL: Language and Coding for Synthesis | 30 |
| **5.** | RTL Design and Verification | 30 |
| **6.** | FPGA Architecture and Prototyping | 30 |
| **7.** | CMOS Logical and Physical Design | 30 |
| **8.** | Project Work | 90 |
|  | Total Hours | 300 |

**6. Detailed Syllabus:**

**a) Introduction to VLSI (30 hours)**

i. What is VLSI? Fundamentals, Advantages of VLSI (5 hours)

ii. Applications of VLSI, Introduction to CMOS (5 hours)

iii. VLSI Design Flow, VLSI Design Style (5 hours)

iv. Concept of Locality, Modularity, Regularity (5 hours)

v. Package technologies and Introduction to CPLD and FPGA (5 hours)

*vi. Assignment Q/A (5 hours)*

**b) Advanced Digital Design (30 hours)**

i. Introduction to digital electronics, Need and applications. (5 hours)

ii. Combinational and Sequential circuits. (5 hours)

iii. Finite State Machines, types and examples. (5 hours)

iv. Glitches and Hazards, Memory Classifications. (5 hours)

v. Asynchronous Sequential Circuits, Design techniques and problems. (5 hours)

*vi. Assignment Q/A ` (5 hours)*

**c) VHDL: Language and Coding for synthesis (30 hours)**

i. Introduction to VHDL, VHDL Applications (5 hours)

ii. VHDL Program structures, operators. (5 hours)

iii. Datatypes in VHDL, Sequential and Concurrent statements. (5 hours)

iv. Functions, Procedure, Simulation: Programs in VHDL (5 hours)

v. Automated Testbench generation, VHDL vs. Verilog. (5 hours)

*vi. Assignment Q/A (5 hours)*

**d) Verilog HDL: Language and Coding for Synthesis (30 hours)**

i. Introduction to Verilog (5 hours)

ii. Types of HDL, Why Verilog HDL? (5 hours)

iii. Hierarchical modeling concepts, Modules and Ports. (5 hours)

iv. Types of Modeling: Gatelevel, Behavioral and Dataflow. (5 hours)

v. Tasks and Functions in Verilog. (5 hours)

vi. Programming in Verilog, *Assignment Q/A (5 hours)*

**e) RTL Design and Verification (30 hours)**

i. Introduction to RTL Design, Need of RTL (5 hours)

ii. RTL Design flow. (5 hours)

iii. Functional Validation and Functional Verification. (5 hours)

iv. Testbench requirements, Compiling Simulation. (5 hours)

v. Waveform Testing and debugging. (5 hours)

*vi. Assignment Q/A (5 hours)*

**f) FPGA Architecture and Prototyping (30 hours)**

i. Difference between ASIC and FPGA (5 hours)

ii. Introduction to FPGA Architecture. (5 hours)

iii. Subparts/Internal blocks of FPGA (5 hours)

iv. Hardware explanation of FPGA. (5 hours)

v. Programming using FPGA’s. (5 hours)

*vi. Assignment Q/A (5 hours)*

**g) CMOS Logical and Physical Design (30 hours)**

i. Introduction to CMOS, Types of CMOS (5 hours)

ii.Fabrication process flow of MOSFET. (5 hours)

iii.Layout design rules. (5 hours)

iv.CMOS Structure, CMOS Biasing. (5 hours)
v.MOSFET C-V Characteristics. (5 hours)

*vi. Assignment Q/A (5 hours)*

**h) Project Work (90 hours)**

 Projects can be made upon – protocols like Router, Serial peripheral Interface, I2C, AMBA-AXI, AHB, APB etc.

**7. Software(s) required:**

1. Xilinx Vivado 2017.

2. Xilinx ISE 14.5 or higher version.

3. Questasim 10.0b or higher version.

**8. Hardware(s) required:**

ZedBoard Zynq -7000 Development Board

**9. Books / Reference material required:**

1. VHDL analysis and modeling of digital systems by Navabi, Zainalabdin, MGH, New York publications.

2. VHDL Primer: By J. Bhasker, PHI Learning, New Delhi

3. Guide to VHDL Syntax: By J. Bhasker

4. FPGA Based System Design: By Wolf, Wayne, Pearson Education

5. Circuit Design with VHDL: By V.A. Pedroni

6. Introduction to Verilog: By Samir Palnitkar

7. Designer’s guide to VHDL - Ashenden, Peter J, Harcourt India, New Delhi

8. CMOS Digital Integrated Circuit analysis and design by Sung Mo Kang.

**10. Job Opportunities after completing this course:**

After completing this course, participants can become:

1. RTL Design Engineer

2. VLSI Design Engineer

3. VLSI Design Team Lead

4. CMOS Design Engineer

5. Frontend Design Engineer

6. VLSI Design Manager

7. EDA Tool Validation Engineer

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