LIST OF PROJECTS

SL.NO	PROJECT TOPIC	NO.OF SLOTS	SKILLS	SUITABLE BRANCHES	DURATION
	Domain: Security Engineering for IoT/VLSI Cryptosystems /Software				
1.	Design & Development of IP Cores for Light Weight Cryptographic Primitives (Encryption / Decryption)	10	Verilog HDL for Hardware IPs	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	4-12 months
			Python/C /MATLAB® for software Tracks	B.Tech /M.Tech in CSE/IT/IS/ECE MCA/MSc (CS/IT/SWE)	
2.	Design & Development of IP Cores for Light Weight Cryptographic Primitives (Integrity)	5	Verilog HDL for Hardware IPs	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	4-12 months
			Python/C /MATLAB® for software Tracks	B.Tech /M.Tech in CSE/IT/IS/ECE MCA/MSc (CS/IT/SWE)	
3.	Design & Development of IP Cores for Light Weight Cryptographic Primitives (Authenticated Encryption)	5	Verilog HDL for Hardware IPs	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	4-12 months
			Python/C /MATLAB® for software Tracks	B.Tech /M.Tech in CSE/IT/IS/ECE MCA/MSc (CS/IT/SWE)	
4.	IoT Solutions for Uploading PNDT forms into database	1	Python/C/ SQL	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
5.	Model Implementation of PNDT database/forms for Ultrasound machine. Investigate various security related issues and implement cryptography techniques for secure communications	1	Python/C/ SQL	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
6.	Implementation of Secured communication module for Indigenous System	1	Python/C/ SQL	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
	Domain: Hardware				
7.	UVM based verification of DBF	1	Verilog/ System verilog	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months

8.	PC Based Automated Hardware Test Jig Development	2	Verilog/C	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
9.	FPGA to FPGA Communication Protocol Development based on SCODEC & CTX	1	Verilog	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
10.	AFE Interface controller for Ultrasound Midend Processor	1	Verilog	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months
11.	Dual Beam former for Ultrasound Imaging	1	Verilog/ Knowledge in DSP	B.Tech /M.Tech in ECE/EEE/CSE/AEI and allied branches	8-12 months