COURSE PROSPECTUS

Name of the Group: VLSI Design Group

Name of the Course: Advanced Diploma - VLSI Physical Design Engineer

Course Code: VL701

Starting Date: 15-May-2019

Duration: 3 Months

Course Coordinator: Sreejeesh SG, +919447769756

Preamble:

VLSI (Very Large Scale Integration) technology has emerged as a very important technology in modern electronics featuring deep sub-micron manufacturing processes, low voltage operations, exploding speeds and smart programmable devices sufficient enough to digest ambient conditions to extremes. The electronics industry worldwide is rapidly approaching another revolutionary leap in the global market scenario. Semiconductor technology has crossed the quarter-micron threshold, making tens of millions of transistors available on a single chip equipped with the powerful arm of VLSI design. This imparts the electronics industry a potential to create designs of incredible densities and lightning speeds while utilizing batteries to power them. This has had a phenomenal impact on widespread applications ranging from consumer electronics, communications, and defense to just about everything.

As part of Electronics India program by Govt. of India, most of the electronic products and semiconductor ICs are planning to make in India. This skill development program in VLSI Physical design will help to generate skilled manpower in IC design and manufacturing.

Objective of the Course:

It is proposed to offer **Advanced Diploma in VLSI Physical Design Engineer** to enable new Electronics graduates/post graduates or working engineers in electronic industries to the concepts used in IC Design, which involves processing, Layout, System Design Methods using Cadence tool. The course will benefit VLSI Engineers seeking lateral shift to a back end job. Engineers looking to work for Block level Physical Design Implementation, Place and Route job domains. This will take VLSI Engineers to a new level known as Physical Design Engineer. The Physical Design Engineer is responsible for converting the circuit design to a geometric representation for manufacturing the integrated circuit (IC).

The main objective of the course is to make individuals understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout

During course work, each individual will get ample time to practice the theory taught in class in the lab sessions.

Outcome of the Course: After successful completion of the course individuals will understand the functional design of IC, converting them into geometric representation to enable Integrated Circuit manufacturing process; verifying and validating the integrated circuit layout. The course will also help to fetch VLSI Physical Design job for job seekers in VLSI area.

Course Structure:

VL701	***Module name***	***Duration***
Module 1	*CMOS Fundamentals, Schematic & Layout*	*One Month*
Module 2	*Digital Physical Design Flow*	*One Month*
Module 3	*Project*	*One Month*

Other Contents

a. **Course Fees** :

General Candidates: Course fee is **Rs 35,000/- including GST**

SC/ST Candidates: Tuition Fees/Examination fees are waived for SC/ST students admitted under SCSP/TSP. However they are required to remit an amount of **Rs.*3500/-* as Advance caution/security deposit**. This amount will be considered as caution/security deposit and will be refunded after successful completion of the course. If the student fails to complete the course successfully this amount along with any other caution/security deposits by the student will be forfeited.

Modular wise Course Fee: Not Applicable for this course

b. **Registration Fee:** An amount of Rs.1000/- (including GST) (nonrefundable) should be paid at the time of registering for the course. **(Registration fee not applicable for SC/ST Students)**
Registration fee not applicable for Certificate courses.

However above the registration fee shall be refunded on few special cases as given below

- Student register and pay fee for more than one course and join for any one course, fee paid for remaining shall be refunded
- Course postponed and new date is not convenient for the student
- Course cancelled in advance, well before the admission date

c. **Course Fee Installment Structure**:

Students can pay the full fees of ***Rs.35, 000/- (including GST)*** in advance or as installments as given below

Fees	***Amount for General Candidates**	**Amount for SC/ST Candidates**	**Due Date (on or before)**
**Advance Fee	Rs. 5000/-	Rs.3500/- (refundable after successful completion of course)	**11th March 2019**
1st Installment	Rs.30,000/- (if advance deposit paid) else Rs.35,000/-	Rs. 3500/- (if not paid advance deposit)	**15th May 2019**

* Above fees is inclusive GST @actuals (*18*%) and rate revision if any will be applicable at the time of payment.

** Advance fee - After publication of first selection list, the students in the first selection list have to pay the Advance Deposit within one week to take the provisional admission. Students in the additional selection should pay both Advance and First installment fee together on or before counseling day

Fine will be applicable to late fee payment as given below

Sl. No.	Description	Fine
1	Late fee payment within two weeks after due date	18% (annually) of the outstanding dues
2	After second week of due date the candidate has to pay readmission fees along with the fine	Readmission fee Rs 250/- plus fine of 18% (annually) of the outstanding dues
3	The candidate has to discontinue the course after third week from the due date	

d. **Eligibility:** **M.E/ M.Tech/ B.E/ B.Tech/ M.Sc in Electrical/ Electronics and Communication/ Electronics and Instrumentation/ Computer Science and allied branches**.

e. Number of Seats : 15
(SC/ST candidates and Persons with disabilities are eligible for seat reservation as per existing rules.)

f. How to Apply :
Students are advised to apply online @http://nielit.gov.in/content/online-registration. Payment towards nonrefundable registration fee of Rs.1,000/- (not applicable for SC/ST students) *may be paid through online payment gateway available in the Registration page or through any of the mode of payments specified in* *http://nielit.gov.in/calicut/content/mode-payments-0*

The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

g. Selection of candidates: *The selection to the course shall be based on the following criteria:*

i. Selection of candidates will be based on their marks in the qualifying examination (i.e. their Btech/Mtech Marks) subject to eligibility and availability of seats.

ii. Knowledge in verilog HDL Programming, C, C++ and Basic Electronics is a pre-requisite of this course.

iii. The list of Provisionally Selected Students will be published in our website **http://nielit.gov.in/calicut** on ***1st March 2019***

iv. All candidates who are provisionally selected have to **pay the full fee or advance fee** on or before ***11th March 2019*** by **direct payment into our account** from any bank where core banking facility is available / or
DD (Drawn in favor of Director, NIELIT, Calicut, Payable at State Bank of India, NITC Branch, Chathamangalam.).

Selected candidates are requested to send the proof of remittance of fee, so as to reach the Centre by ***11th March 2019*****, by email in sreejeesh@nielit.gov.in cc to trng@calicut.nielit.in**

For any queries you may contact the Course Coordinator: Sreejeesh SG Mob: 9447769756 | WhatsApp: 9446711666

v. Payment can be made using the pay in slip available in our web site http://calicut.nielit.in/course/payinslip.pdf through any branch of SBI (where this format is accepted).

h. **Test/Interview**: ***Not Applicable***

i. **Counseling/Admission** : **13th and 14th May 2019**

j. **Spot Admission**: If spot admission is open, spot admission will close within 15 days of Counseling/Admission of a particular course. On spot admission students should provide an undertaking saying that he/she is fully aware that he/she missed so much days of class and will not ask for extra classes or further extension of course.

k. **Admission Procedure :**
Students who have been selected for test/interview/counseling/admission are required to report to the Institute on the prescribed day by 9:30 hrs along with the following
- Original and attested Copies of Proof of Age, Qualifications, etc.
- One passport size photograph
- SC/ST Certificate (Original and two attested copies, if applicable).
- Govt. issued photo ID card (Aadhaar mandatory for SC/ST candidates. Original and one copy)

l. **Discontinuing the course:** No fees (including the caution deposit) under any circumstances, shall be refunded in the event of a student discontinuing the course. No certificate shall be issued for the classes attended.

A student can however, be eligible for module certificates (applicable only for courses which provide for modular admission) which he has successfully completed provided, he/she has paid the entire course fees. This is not applicable to SC/ST candidates availing fee concession. SC/ST candidates availing fee concession are eligible for module certificates only after completing the full course with required attendance

m. **Course Timings** : **9.30 am to 5 pm**

n. **Location and how to reach :**
NIELIT Calicut is located very close to NIT campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses (Buses to NIT via Kunnamangalam) are available from "Palayam Bus Stand and KSRTC Bus Stand". The bus stop at our Institute is called "Panthrand" and is one stop before NIT. The bus fare is around Rs.19/- from Calicut City to NIELIT.

Calicut (Kozhikode) is well connected by Rail, Road and Air form different parts of the country. The maximum and minimum temperatures range between 35^0C and 20^oC.

o. Course enquiries :
Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

p. **Important Dates :**

Events	*Dates*
1st Selection List Publication	*1st March 2019*
Advance Fee payment Last Date	*11th March 2019*
2nd Selection List Publication	*1st May 2019*
Counselling	13th and 14th May 2019
Class Starting	*15th May 2019*

q. **Placement:** visit http://nielit.gov.in/content/placement-3

r. **Hostel facilities :**
Hostel accommodation is available for boys and girls on daily or monthly chargeable basis. The hostel fee varies from Rs.*1400/-* to Rs.*1500* per month depending on the type of accommodation. However, students are required to pay the hostel fees for the duration of the course for which they are seeking admission at the time of joining the course

r. Boarding facilities :
Canteen & Mess facility is available for both boys & girls, students, those who avail mess facility should pay monthly mess fee @Rs.130/*- per day. An amount of Rs.1,000/- should be paid as mess advance to the Canteen Contractor at the time of joining the mess which will be adjusted in the last month mess fee.

**as per the present rate of contract agreement*

An amount of Rs.3,000/- should be paid as caution deposit (hostel & mess) at the time of joining the hostel which will be refunded/adjusted at the end of the course. For students not availing hostel facility, Rs.1,000/- will be the caution deposit

s. Lab Facilities
http://nielit.gov.in/calicut/calicut/content/vlsi-design-group

Course Contents:

Core Modules

Module 1: CMOS Fundamentals, Schematic & Layout – One Month

CMOS Logic Design: MOS Fundamentals, MOS switches and design, Transmission Gates, CMOS Inverter Characteristics, CMOS Combinational and sequential logic. MOS Operation, I-V Characteristics of MOS, Inverter Operation, Nand/Nor CMOS Circuits. Introduction to IC Layout, IC Layout Design Tools

Module 2: Digital Physical Design Flow- One Month

ASIC Design Concepts, ASIC Design Flow-Frontend and backend, EDA tools for Frontend and backend, Introduction to Verilog HDL, Hardware Modeling Overview

a) ***Digital ASIC Design Synthesis:*** Introduction to Digital Synthesis: Synthesize a block-level RTL design to generate a gate-level netlist using Cadence Synthesis Tool.
b) ***Physical Design Flow Setup and Floorplan*** List of inputs (libraries, technology files, netlist, timing constraints, and IO placement) to the PD flow, contents of each input, qualifying the received inputs and sanity checks. Goals of floor planning, different aspects of floor planning, Area estimation, Square/Rectangle/Rectilinear Floorplans, IO placement, macro placement, channel-width estimation, Floor planning guidelines.
c) ***Power Routing & Placement:*** Goals of Power Routing, Types of Power Routing, PG-Rings, PG Mesh and follow-pin/Std cell rail. Goals of Placement, types of placements, pre-place (End-cap, Tap & I/O Buffer) cells, pre-place optimization and in-place optimization, congestion analysis, timing analysis.
d) ***Timing Analysis & Optimization:*** Basic timing checks in digital circuits like Setup Time Violations and Hold Time Violations, understanding timing constraints, timing corners, timing report analysis, general optimization techniques, and typical causes for timing violations and strategies for fixing the same.
e) ***Clock Tree Synthesis (CTS) & Routing:*** What is Clock Tree Synthesis and its Goals, Types of Clock-tree, CTS Specification, Building clock tree, analyze the results, Fine-tuning the Clock-tree and Guidelines for best CTS results. Goals of Routing, Types-of Routing, Global Routing, Detail Routing, Fixing of routing violations (DRC, LVS), and post route optimization.
f) ***ECO Flow & Sign-off Checks:*** What is ECO, Types of ECO, Timing & Functional ECO prep, rolling in the ECO, Performing the ECO placement and routing. Physical Verification (DRC, LVS, ERC), Sign-off Timing analysis.

Project- One Month

1 projects should be taken up covering RTL to GDS flow. We will adopt the industry standard flow for the implementation.