Curriculum

Scheme & Syllabi

for M.Tech Course in

ELECTRONICS DESIGN TECHNOLOGY

of

Kerala Technological University

(With Effect from the Academic Year 2015 onwards)

Scheme of M.Tech. Programme in ELECTRONICS DESIGN TECHNOLOGY

(With Effect from the Academic Year 2015 onwards)

Semester 1 (Credits 23)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks	End Semester Exam		Total Marks	Credits
			L	T	P		Marks	Dur (h)		
1.	EDT 15 101	System Design using Embedded Processors	3	1	0	50	50	3	100	4
2.	EDT 15 102	Advanced Engineering Mathematics	3	1	0	50	50	3	100	4
3.	EDT 15 103	Embedded Programming	3	1	0	50	50	3	100	4
4.	EDT 15 104	Advanced Digital System Design	3	0	0	50	50	3	100	3
5.	EDT 15 105	Elective I	3	0	0	50	50	3	100	3
6.	EDT 15 106	Research Methodology	1	1	0	100	0	0	100	2
7.	EDT 15 107	Seminar	0	0	2	100	0	0	100	2
8.	EDT 15 108	System Design using Embedded Processors - Laboratory	0	0	2	100	0	0	100	1
		Total	**16**	**3**	**4**	**550**	**250**		**800**	**23**
		Elective I					-			
1.	A	Electronic System Design								
2.	B	Wireless Sensor Networks								
3.	C	Advanced Data Communications								
4.	D	Software Engineering								

Semester 2 (Credits 19)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks	End Semester Exam		Total Marks	Credits
			L	T	P		Marks	Dur (h)		
1.	EDT 15 201	Embedded OS & RTOS	3	1	0	50	50	3	100	4
2.	EDT 15 202	High Speed Digital Design	3	0	0	50	50	3	100	3
3.	EDT 15 203	Product Design & Development	3	0	0	50	50	3	100	3
4.	EDT 15 204	Elective - II	3	0	0	50	50	3	100	3
5.	EDT 15 205	Elective - III	3	0	0	50	50	3	100	3
6.	EDT 15 206	Mini Project	0	0	4	100	0	0	100	2
7.	EDT 15 207	Embedded OS & RTOS - Laboratory	0	0	2	100	0	0	100	1
		Total	**15**	**1**	**6**	**450**	**250**		**700**	**19**
		Elective II & III								
1.	A	Internet of Things (IoT)								
2.	B	Multimedia Compression Techniques								
3.	C	Information Security								
4.	D	ASIC & SOC								
5.	E	Design of Digital Signal Processing Systems								
6.	F	Embedded Applications in Power Conversion								
7.	G	Advanced Networking Technologies								
8.	H	Electronic Packaging								

L – Lecture, T- Tutorial, P – Practical

Semester 3 (Credits 14)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks		End Semester Exam		Total Marks	Credits
			L	T	P			Marks	Dur (h)		
1.	EDT 15 301	Elective IV	3	0	0	50		50	3	100	3
2.	EDT 15 302	Elective V	3	0	0	50		50	3	100	3
3.	EDT 15 303	Seminar	0	0	2	100		0	0	100	2
4.	EDT 15 304	Master Research Project Phase I	0	0	16	Guide 20	EC 30	0	0	50	6
		Total	**6**	**0**	**18**	**250**		**100**		**350**	**14**
		Elective IV & V									
1.	A	Wireless Technologies									
2.	B	Automotive Electronics									
3.	C	Mixed Signal System Design									
4.	D	Robotics and Machine Vision									
5.	E	Electronic Instrumentation Design									
6.	F	Advanced Digital Communications									
7.	G	VLSI Signal Processing									
8.	H	Cloud Computing									

Semester 4 (Credits 12)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks			End Semester Exam		Total Marks	Credits
			L	T	P				Marks	Dur (h)		
1.	EDT 15 401	Master Research Project Phase II	0	0	24	Guide 30	Ext expert 30	EC 40	0	0	100	12
		Total	0	0	24	100			0		100	12
		Grand Total				**1350**			**600**		**1950**	**68**

EC-Evaluation Committee, L – Lecture, T- Tutorial, P – Practical

Teaching assistance of 6 hours/week in all semesters for GATE students

Examination Pattern

1. Theory Subjects

The examination pattern for all theory subjects is as given below.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

2. Laboratory Subjects

The details of the internal assessment for each laboratory subject are as given below.

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

3. Seminar/ Mini Projects

Seminar shall be evaluated by the evaluation committee based on the relevance of topic, content depth and breadth, communication skill, question answering etc on the power point presentation of the topic by the student.

Mini Projects shall be evaluated by the evaluation committee based on the working demonstration of the project as well as power point presentation of the same.

FIRST SEMESTER

EDT 15 101 SYSTEM DESIGN USING EMBEDDED PROCESSORS

Maximum Marks – 100; Credits - 4

Modules	Hours
Module 1 **Embedded Concepts** Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools. **ARM Architecture** Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.	10
Module 2 **Overview of Cortex-M3** **Cortex-M3 Basics:** Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. **Instruction Sets:** Assembly Basics, Instruction List, Instruction Descriptions. **Cortex-M3 Implementation Overview:** Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus. **Exceptions:** Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call. **NVIC:** Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer. **Interrupt Behavior:** Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency	12
Module 3	9

Cortex-M3/M4 Programming: **Cortex-M3/M4 Programming:** Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. **Exception Programming:** Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. **Memory Protection Unit and other Cortex-M3 features:** MPU Registers, Setting Up the MPU, Power Management**,** Multiprocessor Communication.	
Module 4 **Cortex-M3/M4 Microcontroller** **STM32L15xxx ARM Cortex M3/M4 Microcontroller:** Memory and Bus Architecture, Power Control, Reset and Clock Control. **STM32L15xxx Peripherals:** GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART. **Development & Debugging Tools:** Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.	8
Tutorial	13
Total Hours	**52**

TEXT BOOKS:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
3. David Seal “ARM Architecture Reference Manual”, 2001 Addison Wesley, England; Morgan Kaufmann Publishers
4. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier.

REFERENCES:

1. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
2. Cortex-M series-ARM Reference Manual
3. Cortex-M3 Technical Reference Manual (TRM)

4. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
5. ARM Company Ltd. “ARM Architecture Reference Manual– ARM DDI 0100E”
6. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).
7. Ajay Deshmukh, “Microcontroller - Theory & Applications”, Tata McGraw Hill
8. Arnold. S. Berger, “Embedded Systems Design - An introduction to Processes, Tools and Techniques”, Easwer Press
9. Raj Kamal, “Microcontroller - Architecture Programming Interfacing and System Design” 1st Edition, Pearson Education
10. P.S Manoharan, P.S. Kannan, “Microcontroller based System Design”, 1st Edition, Scitech Publications

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 102 ADVANCED ENGINEERING MATHEMATICS

Maximum Marks – 100; Credits – 4

Modules	Hours
Module 1 : Linear Algebra Linear Equations and Matrix Algebra: Fields; system of linear equations, and its solution sets; elementary row operations and echelon forms; matrix operations; invertible matrices, LU-factorization Vector Spaces: Vector spaces; subspaces; bases ; dimension; coordinates	10
Module 2 : Linear Transforms Orthogonality: Orthogonal Vectors and Subspaces, Cosines and Projections onto lines, Projections and least squares, Orthogonal Bases and Gram-Schmidt orthogonalization. Linear Systems and Shift invariance, The Laplace Transform, Properties, The Fourier Transform, Properties of Fourier Transform, Fourier Transform of Sequence(Fourier Series) and its properties, Z Transform and its properties.	10
Module3: Digital Transforms and Arithmetic Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, 1D and 2D- DFT, Walsh, Hadamard Transform, Haar Transform, SVD Transform. Digital Arithmetic: Fixed and Floating point representation, IEEE 754 Floating point standards, Floating point arithmetic operations.	10
Module 4: Wavelet Transform Wavelet Transform: Continuous: introduction, C-T wavelets, properties, inverse CWT. Discrete Harr Wavelet Transform and orthogonal wavelet decomposition using Harr Wavelets.	9
Tutorial	13
Total Hours	**52**

TEXT BOOKS:

1. "Linear Algebra and its Applications", David C. Lay, 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005
2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier
3. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi
4. Digital Signal Processing: a practical approach, Emmanuel C Ifeachor, W Barrie Jervis, Pearson Education (Singapore) Pte. Ltd., Delhi

5. Wavelet transforms-Introduction to theory and applications, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education
6. Linear Algebra and its Applications, GilbertStrang.

REFERENCE BOOKS:

1. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists , Murray R. Spiegel, MGH Book Co., New York
2. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK
3. Advanced Engineering Mathematics, JAIN, R K,IYENGAR, S R K, Narosa, NEW YORK
4. Signal processing with fractals: a Wavelet - based approach, Wornell, Gregory, PH, PTR, NEW JERSEY 5. Wavelet a primer, Christian Blatter, Universities press (India) limited, Hyderabad

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 103 EMBEDDED PROGRAMMING

Maximum Marks – 100; Credits - 4

Modules	Hours
Module 1: Embedded OS Fundamentals (Linux) Introduction: Operating System Fundamentals, General Linux Architecture, Linux Kernel, Linux file systems, ROOTFS, Sysfs and Procfs, Embedded Linux: Booting Process in Linux, boot loaders, U-boot, Kernel Images, Linux File systems. GNU Tools: gcc, gdb, gprof, Makefiles	8
Module 2: Embedded C Programming Review of data types –scalar types-Primitive types-Enumerated types-Subranges, Structure types-character strings –arrays- Functions Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly. Embedded programming issues - Reentrancy, Portability, Optimizing and testing embedded C programs. Modelling Language for Embedded Systems: Modeling and Analysis of Real-Time and Embedded systems	10
Module 3: Embedded Applications using Data structures Linear data structures– Stacks and Queues Iimplementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures – Trees and Graphs Object Oriented programming basics using C++ and its relevance in Embedded systems.	12
Module 4: Scripting Languages for Embedded Systems Shell scripting, Programming basics of Python, Comparison of scripting languages	9
Tutorial	13
Total Hours	**52**

Note: Prior knowledge of basic C programming is necessary to study this subject

TEXT BOOKS:

1. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
2. “Embedded C”,Michael J. Pont, Addison Wesley

REFERENCE BOOKS:

1. “Exploring C for Microcontrollers- A Hands on Approach”,Jivan S. Parab, Vinod G. Shelake, Rajanish K.Kamot, and Gourish M.Naik, Springer.
2. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.
3. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education. 3. Steve Heath, “Embedded system design”, Elsevier, 2003.
4. David E. Simon, “An Embedded Software Primer”, Pearson Education, 2003.
5. The Complete Reference C++, Herbert Schildt, TMH
6. C++ programming language, Bjarne Stoustrup,Addison-Wesley
7. GNU C++ For Linux, Tom Swan , Prentice Hall India
8. Object_Oriented programming in C++, Robert Lafore , Galgotia publications
9. Operating System Concepts, Peter B. Galvin, Abraham Silberschatz, Gerg Gagne, Wiley Publishers
10. GNU/LINUX Application Programming, Jones, M Tims

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 104 ADVANCED DIGITAL SYSTEM DESIGN

Maximum Marks – 100; Credits - 3

Topics	Hours
Module 1 **Introduction to Digital Design** Combinational Circuit Design, Synchronous Sequential Circuit Design - Mealy and Moore model, State machine design, Analysis of Synchronous sequential circuit, State equivalence, State Assignment and Reduction, Analysis of Asynchronous Sequential Circuit, flow table reduction, races, state assignment, Design of Asynchronous Sequential Circuit, Designing with PLDs – Overview of PLDs – ROMs, EPROMs – PLA – PAL - Gate Arrays – CPLDs and FPGAs, Designing with ROMs - Programmable Logic Arrays - Programmable Array logic, PAL series 16 & 22 – PAL22V10 - Design examples.	12
Module 2 **VHDL** Basics - Introduction to HDL - Behavioral modeling - Data flow modeling - Structural modeling - Basic language elements – Entity – Architecture - Configurations - Subprograms & operator overloading - Packages and libraries – Test Bench - Advanced Features - Model simulation - Realization of combinational and sequential circuits using HDL – Registers – Flip flops - counters – Shift registers –Multiplexers - sequential machine –Multiplier – Divider, Introduction to Synthesis and Synthesis Issues.	12
Module 3 **Testing, Fault Modelling And Test Generation -** Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Test generation for combinational logic circuits – Testable combinational logic circuit design, Introduction to Design for Testability, BST	7
Module 4 **FPGA** - FPGAs - Logic blocks, Routing architecture, Design flow technology - mapping for FPGAs, Xilinx FPGA Architecture, Xilinx XC4000 - ALTERA's FLEX 8000, Design flow for FPGA Design, Case studies: Virtex II Pro.	8
Total Hours	**39**

TEXT BOOKS:

1. Parag K. Lala, "Digital System Design using programmable Logic Devices", Prentice Hall, NJ, 1994
2. Geoff Bestock, "FPGAs and programmable LSI; A Designers Handbook", Butterworth Heinemann, 1996
3. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.
4. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002
5. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992

REFERENCE BOOKS

1. Jesse H. Jenkins, "Designing with FPGAs and CPLDs", Prentice Hall, NJ,1994
2. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
3. Kevin Skahill, "VHDL for Programmable Logic", Addison -Wesley, 1996
4. Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGRAW-Hill, 1998
5. Digital Circuits and Logic Design – Samuel C. Lee , PHI
6. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
7. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 105 - ELECTIVE I

A - ELECTRONIC SYSTEM DESIGN

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 Practical Analog & Mixed Signal Circuit Design Issues and Techniques: Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components, Op amps: DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier. Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications. Isolation amplifier basics. Active filers: design of low pass, high pass and band pass filters. ADCs and DACs: Characteristics, interfacing to microcontrollers. Selecting an ADC. Power supplies: Characteristics, design of full wave bridge regulated power supply. Circuit layout and grounding in mixed signal system.	10
Module 2 Practical Logic Circuit Design Issues and Techniques: Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices. Electrical behavior (steady state & dynamic) of CMOS& BiCMOS family logic devices. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies. CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations. Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI.	10
Module 3 Electromagnetic Compatibility (EMC): Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems.	9

Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables. Grounding of Electronic Systems: Safety grounds, signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies.	
Module 4 Balancing & Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, system bandwidth. Protection Against Electrostatic Discharges (ESD): Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC. Packaging & Enclosures of Electronic System: Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging's influence and its factors. Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.	10
Total Hours	**39**

TEXT BOOKS:

1. Electronic Instrument Design, 1st edition; by: Kim R.Fowler; Oxford University Press.
2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W.Ott; John Wiley & Sons.
3. Digital Design Principles& Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.
4. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc
5. Intuitive Analog circuit design by: Mark.T Thompson; Published by Elsevier

REFERENCES:

1. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.

2. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ http://www.analog.com
3. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539@ http://www.analog.com
4. Practical Analog Design Techniques; by: Adolofo Garcia and Wes Freeman; Seminar Materials@ http://www.analog.com
5. Selecting An A/D Converter; by:Larry Gaddy; Application bulletin @ http://www.Ti.com
6. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A@ http://www.Ti.com
7. JTAG/IEEE 1149.1 deigns considerations; Application note SCTA029@ http://www.Ti.com
8. Live Insertion; Application note SDYA012@ http://www.Ti.com
9. PCB Design Guidelines For Reduced EMI; Application note SZZA009@ http://www.Ti.com

In addition, National & International journals in the related topics, manufacturer's device data sheets and application notes are to be referred to get practical application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

B - WIRELESS SENSOR NETWORKS

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Issues in Ad Hoc Wireless Networks: Medium Acces Scheme-Routing-Multicasting-Transport Layer Protocols-Self Organization-Security-Addressing and Service Discovery Energy management-Scalability-Deployment Considerations, Ad Hoc Wireless Internet. Sensor Networks Comparison with Adhoc wireless networks-Challenges for WSNs - Difference between sensor networks and Traditional sensor networks –Types of Applications –Enabling Technologies for Wireless Sensor Networks –Single Node Architectures –Hardware Components – Energy Consumption of Sensor Nodes, Issues in Designing a Multicast Routing Protocol. OS for WSN.	12
Module 2: Sensor Network Architecture Data Dissemination-Flooding and Gossiping-Data gathering Sensor Network Scenarios –Optimization Goals and Figures of Merit – Design Principles for WSNs- Gateway Concepts – Need for gateway – WSN to Internet Communication – Internet to WSN Communication –WSN Tunneling.	9
Module 3: MAC Protocols MAC Protocols for Sensor Networks -Location Discovery-Quality of Sensor Networks-Evolving Standards-Other Issues- Low duty cycle and wake up concepts- The IEEE 802.15.4 MAC Protocols Energy Efficiency -Geographic Routing Mobile nodes	9
Module 4: Routing Gossiping and Agent based Unicast Forwarding-Energy Efficient Unicast-Broadcast and Multicast Geographic Routing-Mobile nodes-Security-Application Specific Support - Target detection and tracking-Contour/ edge detection-Field Sampling.	9
Total Hours	**39**

TEXT BOOKS:

1. Holger Karl and Andreas Wiilig, “Protocols and Architectures for Wireless Sensor Networks” John Wiley & Sons Limited 2008.
2. I.F .Akyildiz and Weillian, “A Survey on Sensor Networks”,IEEE Communication Magazine, August 2007.

REFERENCES:

1. Wilson , “Sensor Technology hand book,” Elsevier publications 2005.
2. Anna Hac “Wireless Sensor Networks Design,” John Wiley& Sons Limited Publications 2003.
3. C.Siva Ram Murthy and B.S.Manoj “Ad Hoc Wireless Networks,” Pearson Edition 2005.

In addition, manufacturers Device data sheets, IEEE publications and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

C - ADVANCED DATA COMMUNICATIONS

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Digital Modulation Schemes: BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery. Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, SMDS Switching: Circuit Switching, Packet Switching, Message Switching. Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.	11
Module 2: Basic Concepts of Data Communications, Interfaces and Modems: Data Communication Networks, Protocols and Standards, CAN, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/IP Protocol suite and Comparison with OSI model.IPV4 and IPV6.	10
Module 3: Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code Data Link Control: Line Discipline, Flow Control, Error Control Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.	10
Module 4: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access-ReservationPolling- Token Passing, Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA), OFDM and OFDMA.	8
Total Hours	**39**

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI

REFERENCES:

1. Data and Computer Communications - William Stallings, 8th Ed., 2007, PHI.
2. Data Communication and Tele Processing Systems -T. Housely, 2nd Ed, 2008, BSP.
3. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2005, PHI.
4. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

D - SOFTWARE ENGINEERING

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 - Introduction What is Software Engineering, The Software Process: Software life cycle models Software Requirements: Functional and non-functional requirements, user requirements, system requirements, SRS. Requirements Engineering Processes: Feasibility studies, elicitation and analysis, validation, management. System Models: Content model, Data model, Behavioral model, Object Model	10
Module 2 - Architectural Design System structuring, control models, modular decomposition, domain-specific architectures, distributed systems architecture. Object-oriented Design: Objects and classes, Object oriented design using UML. Real-time Software Design: System design, real time executives. Design with Reuse: Component-based development, application families, designs patterns. User Interface Design: Design principles, user interaction, information presentation, user support, interface evaluation.	10
Module 3 - Implementation and Testing Choice of programming languages Verification and Validation, Software Testing: Unit testing, Integration Testing, Validation testing, Systems testing Software Maintenance: Legacy systems, software change, software re-engineering, Reverse Engineering.	10
Module 4 Software Project Management: Project planning, scheduling, risk management.. Software Cost Estimation: Productivity estimation techniques, algorithmic cost modeling, project duration and staffing. Process Improvement: Process and product quality, process analysis and modeling, process measurement, process CMM.	9
Total Hours	**39**

TEXT BOOKS:

1. R. S. Pressman, *Software Engineering*, 6/e, McGraw Hill, 2002.
2. Ian Sommerville, *Software Engineering*, 6/e, Pearson Education Asia, 2001.
3. Shari Pfleeger, Software Engineering:Theory and Practice, Pearson Education 2001.
4. P. Jalote, *An Integrated Approach to Software Engineering*, Narosa, 1993.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 106 RESEARCH METHODOLOGY

Maximum Marks – 100; Credits - 2

Modules	Hours
Module 1 **Research Methodology: An Introduction** Meaning of Research Objectives of Research Motivation in Research Applications of Research Definition of Research Characteristics of Research Types of Research Steps in Research Process **Formulating a Research Problem** Reviewing the Literature Formulating a Research Problem Identifying Variables Constructing Hypothesis	7
Module 2 **Conceptualising a research design** Definition of a Research Design Need for Research Design Functions of Research Design Features of a Good Design **Methods of Data Collection** Collection of Primary Data Observation Method Interview Method Collection of Data through Questionnaires Collection of Data through Schedules	7
Module 3 **Processing and Analysis of Data** Processing Operations Elements/Types of Analysis Statistics in Research Measures of Central Tendency Measures of Dispersion Measures of Asymmetry (Skewness)	7

Writing a Research Report Research writing in general Referencing Writing a Bibliography Developing an outline Writing about a variable	
Module 4 Interpretation of Data and Paper Writing – Layout of a Research Paper, Journals in Computer Science, Impact factor of Journals, When and where to publish ? Ethical issues related to publishing, Plagiarism and Self-Plagiarism **A study of the use of the following tools** Matlab / Simulink LaTeX/ MS Office	5
Total Hours	**26**

TEXT BOOKS:

1. Ranjit Kumar, "Research Methodology: A Step-by-step Guide for Beginners", Pearson, Second Edition
2. Kothari, C.R, "Research Methodology : Methods and Techniques", New age International publishers

REFERENCE BOOKS:

1. Sanjit K. Mitra, "Digital Signal Processing Laboratory Using MATLAB" , Mcgraw-Hill College, ISBN-13: 978-0073108582
2. Rudra Pratap, "Getting Started with MATLAB: Version 6: A Quick Introduction for Scientists and Engineers", 2001, Oxford University Press
3. Wayne Goddard and Stuart Melville, "Research Methodology : An Introduction", 2nd Edition, 2001, Juta & Co Ltd

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Mid Term Internal Test	40 Marks
Assignment I	10 Marks
Assignment II	10 Marks
Final Internal Test	40 Marks
Total	**100 Marks**

EDT 15 107 SEMINAR

SEMINAR	Max marks - 100; Hours/week: 2	Credits: 2

	Hours
Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.	Per week 2
Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 15 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.	
Internal continuous assessment: 100 marks	

Subject Relevance	:	10 marks
Concept/ Knowledge in the topic	:	20 marks
Presentation	:	40 marks
Report	:	30 marks
Total marks	:	**100 marks**

EDT 15 108 SYSTEM DESIGN USING EMBEDDED PROCESSORS - LABORATORY

Maximum Marks – 100; Credits – 1

		Hours
	Module 1 – ARM Assembly Programming	7
1.	Write a program to add two 32-bit numbers stored in r0 and r1 registers and write the result to r2. The result is stored to a memory location. a) Run the program with breakpoint and verify the result b) Run the program with stepping and verify the content of registers at each stage	
2.	For the following values of *a* and *b*, predict the values of the N, Z, V, and C flags produced by performing the operation *a* + *b*. Load these values into two ARM registers and modify the program created in above question1 to perform an addition of the two registers. Using the debugger, record the flags after each addition and compare those results with your predictions. Values of a => 1) 0xFFFF0000 2) 0xFFFFFFFF 3) 0x67654321 Values of b => 1) + 0x87654321 2) + 0x12345678 3)+ 0x23110000	
3.	Write a program to multiply two 16-bit numbers stored in r0 and r1 registers and write the result to r3. Put 0xFFFFFFFF and 0x80000000 into the source registers and verify the result.	
4.	Write an ARM code to implement the following register swap algorithm using only two registers. a) Using arithmetic instructions b) Using logical instructions	
5.	Write ARM assembly to perform the function of absolute value. Register r0 contains the initial value, and r1 contains the absolute value.	
6.	Write ARM assembly to perform the function of division. Registers r1 and r2 contain the dividend and divisor, r3 contains the quotient, and r5 contains the remainder.	
7.	Write ARM assembly to perform the following array assignment in C: for (i = 0; i <= 10; i++) {a[i] = b[i] + c;} Assume that r3 contains *i*, r4 contains *c*, the starting address of array *a* is in r1, and the starting address of array *b* is in r2.	
	Module 2 - Embedded C Programming on ARM Cortex M3/M4 Microcontroller	7
1.	Write a program to turn on green LED (Port B.6) and Blue LED (Port B.7) on STM32L-Discovery by configuring GPIO.	

2.	Write a program to toggle green LED (Port B.6) and Blue LED (Port B.7) on STM32L-Discovery by configuring GPIO and using software delays.	
3.	Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec. Use Timer3 in polling method for delay generation.	
4.	Transmit a string "Programming with ARM Cortex" to PC by configuring the registers of USART2. Use polling method.	
5.	Transmit a string "Programming with ARM Cortex" to PC by configuring the registers of USART3. Use polling method.	
	Module 3 - ARM Cortex M3/M4 Programming with CMSIS	5
1.	Write a program to toggle the LEDs at the rate of 1 sec using standard peripheral library. Use Timer3 for Delay.	
2.	Transmit a string "Programming with ARM Cortex" to PC by using standard peripheral library with the help of USART3. Use polling method.	
3.	Receive the data send by PC, compare it with threshold and switch on the Green LED if below threshold and Red LED if above.	
4.	Write a program to read the analog input connected to ADC and compare with threshold so as to control the Digital outputs (LEDs). Use standard peripheral library and interrupt method.	
5.	Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec using Timer2 in interrupt configuration.	
6.	Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec using Timer3in interrupt configuration.	
7.	Transmit a data to PC by using standard peripheral library with USART1. Use interrupts method.	
8.	Receive a data sent by PC by using standard peripheral library with USART1. Use interrupts method.	
	Module 4 - ARM Cortex M3/M4 Peripherals	7
1.	**Design of a real-time data acquisition & control system using the STM32Lxx ARM Cortex M3 Microcontroller** It is required to monitor and control the temperature in a boiler which ranges from 0°C to 100°C every **1second** using the STM32Lxx ARM Cortex M3 Microcontroller. The temperature has to be kept at a set-point of 50°C ± 2°C. The temperature is measured through an RTD sensor and is transmitted through a 4-20 mA two wire transmitter. The 4-20mA is converted to 1 to 5V by 250 ohm terminating resistor. 1 to 5V is available at the analog input port. 1V corresponds to 0°C and 5V corresponds to 100°C. An ON/OFF relay connected to A PIO Port bit is used to control the heater element. A PC is used as the monitoring and control station. Read the data through ADC and send the data from 0V to 5V in steps of 0.1V. The same has to be repeated after reaching the maximum value of 5V.	

1. The temperature has to be sent to the PC every 1 second in the following protocol format and the same has to be displayed using the LAS software in WISE-96 on the PC.

STX	**MSL**	**CMD**	**SCMD**	**DATA_LO**	**DATA_HI**	**ETX**
byte 1	byte 2	byte 3	byte 4	byte 5	byte 6	byte 7

STX	:	Start of Text	02H
MSL	:	Message length, in bytes	
CMD	:	Command byte	90H
SCMD	:	Sub-command byte	00H (Channel no)
DATA_LO	:	Lower byte of data word	
DATA_HI	:	Upper byte of data word	
ETX	:	End of Text	03H

2. Provision should be given for receiving the set-point value of temperature from the PC, and the set point is to be framed in the above protocol format.
3. If the transmitter is switched off or if it sends invalid data, i.e, below 4mA, an error message packet similar to the above one with CMD byte set to 95H should be send to the PC, instead of the data packet.

   Hint: Use a Trimpot to apply the voltage. Use an LED to display the ON/OFF status. ON/OFF control strategy can be used for controlling the power supplied to the heater.

	Total Hours	26

Software used: Keil Microvision IDE, 'C' Compiler and Assembler for ARM.

Platforms used: PC, STM32L15xxx ARM Cortex M3/M4 Microcontroller Discovery Kits

REFERENCES:

1. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
2. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
3. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers
4. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", 2006, Elsevier.
5. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education.
6. Cortex-M series-ARM Reference Manual
7. Cortex-M3 Technical Reference Manual (TRM)
8. ARM Company Ltd. "ARM Architecture Reference Manual– ARM DDI 0100E"

9. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
10. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).

Internal Continuous Assessment: 100 marks

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

SECOND SEMESTER

EDT 15 201 EMBEDDED OS & RTOS

Maximum Marks – 100; Credits - 4

Modules	Hours
Module 1 - Embedded OS (Linux) Internals Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication - Semaphore, Pipes, FIFO, Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling. Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network	12
Module 2 – Open source RTOS Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS. POSIX standards, RTOS Issues - Selecting a Real Time Operating System, RTOS comparative study. Converting a normal Linux kernel to real time kernel, Xenomai basics. Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.	12
Module 3 – VxWorks / Free RTOS **VxWorks/ Free RTOS** Scheduling and Task Management - Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems - General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral	8
Module 4 – Case study Cross compilers, debugging Techniques, Creation of binaries **& porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar),** Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board	7
Tutorial	13
Total Hours	**52**

TEXT BOOKS:

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan
2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein
3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

REFERENCES:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
4. Real-time Systems – Jane Liu, PH 2000
5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A
6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J
7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J
8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J
9. Monitoring and Debugging of Distributed Real-Time Systems: TSAI, Jeffrey J P & Yang, J H
10. Embedded Software Primer: Simon, David E.
11. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 202 - HIGH SPEED DIGITAL DESIGN

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 **Introduction to high speed digital design.** Frequency, time and distance - Capacitance and inductance effects - High seed properties of logic gates - Speed and power -Modelling of wires -Geometry and electrical properties of wires - Electrical models of wires - transmission lines - lossless LC transmission lines - lossy LRC transmission lines - special transmission lines	10
Module 2 **Power distribution and noise** Power supply network - local power regulation - IR drops - area bonding - onchip bypass capacitors - symbiotic bypass capacitors - power supply isolation - Noise sources in digital system - power supply noise - cross talk - intersymbol interference	8
Module 3 **Signalling convention and circuits** Signalling modes for transmission lines -signalling over lumped transmission media - signalling over RC interconnect - driving lossy LC lines - simultaneous bi-directional signalling - terminations - transmitter and receiver circuits	9
Module 4: **Timing convention and synchronisation** Timing fundamentals - timing properties of clocked storage elements - signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - synchronization failure and metastability - PLL and DLL based clock aligners	12
Total Hours	**39**

TEXT BOOKS:

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic by",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by ", Wiley , 2007
3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006
4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 203 PRODUCT DESIGN & DEVELOPMENT

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 - Product Design and Development: I Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design.	10
Module 2 - Product Design and Development: II Design for Manufacturing (DFM), Prototyping, Robust Design, Patents and Intellectual property, Product Development Economics, Managing Product Development Projects.	10
Module 3 - Quality Management Principles Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement, SPC, Quality Systems, Bench Marking.	10
Module 4 - Quality Management Tools Quality Function Deployment, Failure Mode and Effect Analysis, Management Tools.	9
Total Hours	39

Note:
Tutorial sessions include Group Discussions and Team Work

TEXT BOOKS

1. Total Quality Management; Third edition By: Dale H. Besterfield, Pearson Education Asia
2. Product Design & Development; Third edition By: Karl T Ulrich & Steven D Eppinger; Mc Graw Hill

In addition, relevant papers in journals & articles etc. are to be referred to get further information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 204 - ELECTIVE II
&
EDT 15 205 - ELECTIVE III

A. INTERNET OF THINGS (IoT)

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: The IoT Networking Core : Technologies involved in IoT Development: **Internet/Web and Networking Basics** OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing **IoT Platform overview** Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.	12
Module 2: IoT Architecture: History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols **Applications:** Remote Monitoring & Sensing, Remote Controlling,Performance Analysis **The Architecture** The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN **Security aspects in IoT**	8
Module 3: IoT Application Development: **Application Protocols** MQTT, REST/HTTP, CoAP, MySQL	13

Back-end Application Designing Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS App Development tools	
Module 4: Case Study & advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)	6
Total Hours	**39**

Note: Prior knowledge of basic Wireless & Networking, Wireless Sensor Networks, C programming, Embedded OS is necessary to study this sub

TEXT BOOKS:

1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers
3. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann

REFERENCES:

1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
2. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , Arshdeep Bahga
3. Designing the Internet of Things , Adrian McEwen (Author), Hakim Cassimally
4. Asoke K Talukder and Roopa R Yavagal, “Mobile Computing,” Tata McGraw Hill, 2010.
5. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition
6. Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 6th Edition
7. F. Adelstein and S.K.S. Gupta, “Fundamentals of Mobile and Pervasive Computing,” McGraw Hill, 2009.
8. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010

9. Cloud Security: A Comprehensive Guide to Secure Cloud Computing, Ronald L. Krutz, Russell Dean Vines, Wiley-India, 2010

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

B - MULTIMEDIA COMPRESSION TECHNIQUES

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 - Introduction Special features of Multimedia – Graphics and Image Data Representations – Fundamental Concepts in Video and Digital Audio – Storage requirements for multimedia applications -Need for Compression - Taxonomy of compression techniques – Overview of source coding **Text Compression** Compaction techniques – Huffman coding – Adaptive Huffman Coding – Arithmetic coding – Shannon-Fano coding – Dictionary techniques – LZW family algorithms.	9
Module 2 - IMAGE COMPRESSION Transform Coding – Discrete Cosine Transform(DCT), Quantization and Coding of Transform Coefficients. JPEG Standard – Sub-band coding algorithms: Design of Filter banks – Wavelet based compression: Implementation using filters – EZW, SPIHT coders – JPEG 2000 standard.	10
Module 3 - AUDIO COMPRESSION Audio compression techniques - μ- Law and A- Law companding. Frequency domain and filtering – Basic sub-band coding – Application to speech coding – G.722 – Application to audio coding – MPEG audio. Speech compression techniques – LPC and CELP.	10
Module 4 - VIDEO COMPRESSION Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II: MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – Packet Video. Multimedia Delivery-Multiplexing, Packetization, Time stamping, Synchronization and playback.	10
Total Hours	**39**

TEXT BOOKS:

1. Khalid Sayood: Introduction to Data Compression, Morgan Kauffman Harcourt India, 3rd Edition, 2010
2. David Salomon: Data Compression – The Complete Reference, Springer Verlag New York Inc., 4th Edition, 2006.

REFERENCES:

1. Yun Q. Shi, Huifang Sun: Image and Video Compression for Multimedia Engineering - Fundamentals, Algorithms & Standards, CRC press, 2003.
2. Peter Symes: Digital Video Compression, McGraw Hill Pub., 2004.
3. Mark Nelson: Data compression, BPB Publishers, New Delhi, 2008
4. Mark S. Drew, Ze-Nian Li: Fundamentals of Multimedia, PHI, 1st Edition, 2009.
5. Watkinson, J: Compression in Video and Audio, Focal press, London.1995.
6. Jan Vozer: Video Compression for Multimedia, AP Profes, NewYork, 1995
7. Gonzalez and Woods, Digital Image Processing, 3rd Ed, PHI

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

C - INFORMATION SECURITY

Maximum Marks – 100; Credits - 3

Modules	Hours
Module I - Cryptography Introduction to Cryptography: OSI Security Architecture - Security Services, Security Attacks, Security Mechanism. Introduction to Classical Cryptography. Modern Cryptography: Secret key Cryptography - DES, AES. Public key Cryptography - Diffie-Hellman, RSA, ECC. Introduction to Hash Algorithm, Introduction to Digital Signature, Introduction to PKI.	10
Module II – System Security Introduction - Access Control, Intrusion Detection and Prevention. Firewalls: Firewall Design Principles - Firewall Characteristics, Types of Firewalls. Trusted System. Malicious Soft wares: Virus, Trojan Horse, Ad ware/ Spy ware, Worms, Logic Bomb. Cyber Law and Forensics - IT ACT 2000, Cyber Forensics.	7
Module III - Network Security Introduction to Network Concepts, OSI Layers and Protocols, Network Devices, Network layer Security (IPSec) - IP Security Overview, IPSec Architecture, Authentication header, Encapsulating security Payload, Combining Security Associations, Key management. Transport Layer Security - SSL/TLS, SET. Application Layer Security - Authentication Applications, Kerberos, X. 509 Authentication Services. E-mail Security – PGP, S/MIME.	14
Module IV – Embedded Security Introduction, Types of Security Features – Physical, Cryptographic, Platform. Kinds of Devices – CDC, CLDC. Embedded Security Design, Keep It Simple and Stupid Principle, Modularity Is Key, Important Rules in Protocol Design, Miniaturization of security, Wireless Security, Security in WSN.	8
Total Hours	**39**

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice- William Stallings
2. Practical Embedded Security: Building Secure Resource Constrained Systems - Timothy Stapko, Publisher Newnes.

REFERENCE BOOKS:

1. Cryptography: Theory and Practice – 3rd Ed. SD Stinson, CRC Press.
2. Information Security for Technical Staff-SEI.
3. Guide to firewalls & network security: with intrusion detection & VPNs- HOLDEN, GREG.
4. CISSP: Certified Information Systems Security Professional Study Guide- Stewart, James Michael Et Al.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

D - ASIC AND SOC

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 **Types of ASICs** – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.	10
Module 2 **ASIC Library design:** Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC, ASIC Construction – Floor planning & placement – Routing	8
Module 3 **System on Chip Design Process:** A canonical SoC design, SoC Design Flow – Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process, System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies. MPSoCs. Techniques for designing MPSoCs	12
Module 4 **SoC Verification**: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.	9
Total Hours	**39**

TEXT BOOKS:

1. “SoC Verification-Methodology and Techniques”, Prakash Rashinkar, Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.
2. “Reuse Methodology manual for System-On-A-Chip Designs”, Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001
3. Smith, "Application Specific Integrated Circuits", Addison-Wesley,2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

E - DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Introduction to Digital Signal Processing Signals in Time and Frequency Domains Signals and Filtering Architecture of ARM Cortex M3/M4 Processor. ADC/ DAC Interfacing to ARM Cortex M3/M4 Processor Introduction to MATLAB and SIMULINK	9
Module 2 - Digital Signal Processing Algorithms: Filter Design: FIR Digital filter design. Frequency Domain Fourier Transform: DFT, FFT, Spectral Analysis DTMF	10
Module 3 - Digital Signal Processing Application: Real-time Implementation: Real-time Implementation of FIR Digital filter using ARM Cortex M3/M4 Processor. Real-time Implementation of Fast Fourier Transform applications using ARM Cortex M3/M4 Processor. Implementation of DTMF Tone Generation and Detection ARM Cortex M3/M4 Processor.	10
Module 4 - Current trends in Digital Signal Processor: FPGA Technology DSP Technology Requirements Design implementation Multiply Accumulator (MAC) and Sum of Product (SOP) Implementation of Serial/Parallel Convolver using FPGAs FPGA Based DSP System Design FIR filters FIR Theory	10

Designing FIR filters Direct Window Design method Constant Coefficient FIR Design Direct FIR Design Cooley-Tukey FFT Algorithm implementation using FPGA	
Total Hours	**39**

TEXT BOOKS:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition; by: Naim Dahnoun
2. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010
3. DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition; by: Rulph Chassaing
4. Digital Signal Processing: A System Design Approach, 1st Edition; by: David J Defatta J, Lucas Joseph G & Hodkiss William S; John Wiley
5. Digital Signal Processing with Field Programmable Gate Arrays: 2nd Edition, by: U. Meyer – Base, Springer

REFERENCES:

1. Real - Time Digital Signal Processing: Implementations, Applications, and Experiments with the TMS320C55X, Kuo, Sen M, Lee, Bob H, John Wiley & Sons Ltd.
2. Digital Signal Processing, Third Edition, Sanjit K. Mitra, Tata McGraw Hill
3. Digital Signal Processing – A Practical Guide for Engineers and Scientists, Steven W Smith, Elsevier
4. Digital Signal Processing - A Student Guide, 1st Edition; by: T.J. Terrel and Lik-Kwan Shark; Macmillan Press; Ltd.
5. Sen M.Kuo , Woon-Seng S. Gan, *Digal Signal Processors: Architectures, Implementations, and Applications* Prentice Hall 2004.
6. Keshab K. Parhi, *VLSI Signal Processing Systems, Design and Implementation*, John Wiley & Sons,1999.
7. Digital Signal Processing Laboratory, B. Preetham Kumar, Taylor & Francis, CCS DSP Applications
8. Introduction to Digital Signal Processing, 1st Edition; by: John G Proakis, Dimitris G Manolakis
9. Digital Signal Processing Design, 1st Edition; by: Andrew Bateman, Warren Yates
10. A Simple approach to Digital Signal processing, 1st Edition; by: Kreig Marven & Gillian Ewers; Wiely Interscience
11. DSP FIRST - A Multimedia Approach, 1st Edition; by: JAMES H. McClellan, Ronald Schaffer and Mark A. Yoder; Prentice Hall
12. Signal Processing First, 1st edition; by: James H. McClellan, Ronald W. Schafer and Mark A. Yoder; Pearson Education

13. Digital Signal Processing, 1st Edition; by: Oppenheim A.V and Schafer R.W; PH
14. Digital Processing of Speech Signals, 1st Edition; by: L.R. Rabiner and Schafer R.W; PH
15. Digital Signal Processing – Architecture, Programming and Applications, by: B. Venkataramani & M.Bhaskar; Tata McGraw Hill
16. A Practical Approach to Digital Signal Processing, by: K. Padmanabhan, S. Ananthi & R.Vijayarajeswaran; New Age International Publishers
17. Theory & Application of Digital Signal Processing, 1st Edition; by: Rabiner L.R & Gold B; PH
18. Digital Signal Processing, 1st Edition; by: P Ramesh Babu,

In addition, National/ International journals in the field, manufacturers Device data sheets and application notes and research papers in journals are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

F - EMBEDDED APPLICATIONS IN POWER CONVERSION

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 Power Converters: Power converter system design. Isolated and Non-isolated dc-dc converters. Inverters with square and sinusoidal output. PWM switching – unipolar and bipolar, sine PWM Practical Converter design considerations: Power semiconductor devices – Power Diodes, BJT, MOSFET, IGBT. MOSFET & IGBT – Ratings, SOA, Switching characteristics, Gate Charge, Paralleling devices. Dos and Don'ts of using Power MOSFETs, Gate drive characteristics & requirements of power MOSFETs and IGBT modules. Design of turn on and turn off snubbers. Magnetic components: Design of high frequency transformer, design of Inductors, design of CTs.	10
Module 2 Design of controllers for Power converters: Micro controllers and DSP based controllers for power conversion. Peripheral interfacing - ADC, Keyboard, LCD display, PWM generation. Design of PWM bridge controller based on low end and high-end controllers. Interfacing of controller output to power module. Designs based on dedicated gate driver ICs. Design of isolated gate drives.	9
Module 3 Design of UPS: Online, off line UPS. Operation & design criteria of AC switch, Operation & design criteria of battery charger, operation & design criteria of inverter, active PFC circuits. Thermal design of power converters.	10
Module 4 DC Motor Drives: Design of adjustable speed DC motor drives, speed control of a separately excited motor, design of closed loop control, design chopper controlled DC motor drive, design of four quadrant chopper. AC Motor Drives: Design of 3 phase PWM VSI inverter, design of v/f control for induction Motor, design of open loop and closed loop control. Vector control of AC motors, space vectors, vector control strategy for induction motor.	10
Total Hours	**39**

TEXT BOOKS

1. Power Electronics; By: Mohan, Underland, Robbins; John Wiley & Sons
2. Simplified design of Switching Power supplies; By: John D Lenk; EDN series for designers.
3. Design of magnetic components for switched mode power converters; By L Umanad, S.R Bhat; Wiely Eastern ltd.

REFERENCES

1. MOSFET& IGBT Designers manual, International Rectifier
2. UPS design guide, International Rectifier

In addition, relevant papers in journals & articles etc. are to be referred to get further information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

G - ADVANCED NETWORKING TECHNOLOGIES

Maximum Marks – 100; Credits - 3

Modules	Hours
Module I Troubleshooting and Management – Host Configuration, Connectivity, Testing Path Characteristics, Packet Capture, Device Discovery and Mapping – Troubleshooting Strategies – Components – Bridges, Routers and Switches – Network OS – Novel Netware, Linux.	10
Module II IP next generation – Addressing, Configuration, Security, QOS - VOIP- Issues in VOIP – Distributed Computing and Embedded System – Ubiquitous Computing - VPN.- Understanding Storage Networking – Storage Networking Architecture – The Storage in Storage Networking, The Network in Storage Networking, Basic Software for Storage Networking – SAN Implementation Strategies.	10
Module III WDM – WDM Network Design – Control and Management – IP Over WDM – Photonic Packet Switching.	10
Module IV Monitoring and Control – SNMP, V2, V3, RMON, RMON2.	9
	39

REFERENCES

1. John D. Sloan, “Network Troubleshooting”, Aug’2001 – O’Reilly.
2. Radic Perlman, “Interconnections: Bridges, Routers, Switches and Internetworking Protocols”, Second Edition, Addison Wesley professional, 1999.
3. Andrew S. Tanenbaum, “Modern operating system”, Pearson Education
4. Silvano gai, “Internetworking IPV6 with CISCO Routers”, McGraw– Hill computer communication series.
5. Tom Clark,” Designing Storage Area Network: A practical reference for implementing fiber channel and IP SAN’s”, Second Edition, Addison Wesley professional, 2003.
6. Richard M Barker Paul Massiglia – John Wiley & Sons Inc., “Storage Area Network Essentials: A complete guide to understanding and implementing SANS“, 2001.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

H - ELECTRONIC PACKAGING

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Overview of electronic systems packaging, Definition of a system and history of semiconductors , Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications , Definition of PWB. Video on "Sand-to-Silicon" ,Wafer fabrication, inspection and testing , Wafer packaging; Packaging evolution; Chip connection choices , Wire bonding, TAB and flipchip-1 ,Wire bonding, TAB and flipchip-2.	8
Module 2: Necessary of packaging. Types , Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging , Multichip modules (MCM)-types; System-inpackage (SIP);Packaging roadmaps; Hybrid circuits; Electrical Issues – I; Resistive Parasitic , Electrical Issues – II; Capacitive and Inductive Parasitic , Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.	10
Module 3: Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights , Design Flow considerations; Beginning a circuit design with schematic work and component layout , Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for Reliability. Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued; Video highlights; Surface preparation, Photoresist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; Resist stripping; Screen-printing technology, Through-hole manufacture process steps; Panel and pattern plating methods. Video highlights on manufacturing; Solder mask for PWBs; Multilayer PWBs; Introduction to microvias, Microvia technology and Sequential build-up technology process flow for high-density interconnects, Conventional Vs HDI technologies; Flexible circuits; Tutorial session.	11

Module 4: SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave solderin, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues. Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.	10
Total Hours	**39**

TEXT BOOKS:

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001.

REFERENCES:

1. William D.Brown,Advanced Electronic Packaging, IEEE Press, 1999.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 206 MINI PROJECT

Maximum Marks – 100; Credits – 2

The students can select hardware, software or system level mini projects. The mini project can be implemented using **Microcontroller or DSP or FPGA or RTOS** tools which they have studied. A complete product or project can be selected. The project can be done individually or as a group of two students.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of evaluation, demonstration, presentation etc. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Attendance & Regularity	20 Marks
Evaluation I	30 Marks
Evaluation II	30 Marks
Assessment by Guide	20 Marks
Total	**100 Marks**

EDT 15 207 - EMBEDDED OS & RTOS - LABORATORY

Maximum Marks – 100; Credits – 1

	Hours
Module 1 - Embedded OS (Linux) Experiments are given in annexure 1. A minimum of 6 experiments from the file, process and I/O management should be taken up.	6
Module 2 - RTOS Inter Process Communication (IPC) experiments given in annexure 2 should be taken up. A minimum of 6 experiments should be taken up.	6
Module 3 - VxWorks / Free RTOS Minimum of seven experiments from Scheduling and Task Management and three experiments from I/O Management should be taken up. A minimum of 10 experiments should be taken up.	6
Module 4 - RTLinux Experiments are given in annexure 4. A minimum of 10 experiments from RTLinux assignment 1, covering RTthreads, IPC, semaphore etc should be done. Case study using Vxworks/ RTLinux RTOS: 1. Implement the Embedded Linux porting on ARM Cortex boards and develop an application under Linux environment for ARM architecture. 2. Design and Implement a Device Driver for standard Serial Port using PC and implement a data acquisition system with the following features. Analog values of physical parameters such as Temperature, Pressure etc. to be read from an ADC using the Microcontroller and process the data and send the data to another PC. The data has to be displayed in the PC. In case of the parameters above the set point, an Alarm has to be generated and the same has to be implemented in a Microcontroller by switching OFF an LED or a Relay. The set point for each parameter has to be sent from the second PC.	8
Total Hours	**26**

Platforms used: PC Pentium is the target for VxWorks and RTLinux

Software used: VxWorks/ Free RTOS, RTLinux

REFERENCES:

1. GNU/LINUX Application Programming, Jones, M Tims, DREAMTECH PRESS, NEW DELHI
2. Embedded /Real-Time Systems: Concepts, Design and Programming—The Ultimate Reference, Prasad K.V.K.K, DREAMTECH PRESS, NEW DELHI
3. VxWorks Programmers guide
4. VxWorks Reference manual
5. Tornado API Programmers guide
6. Tornado Users guide
7. Embedded Linux®: Hardware, Software, and Interfacing, By Craig Hollabaugh Ph.D., Addison Wesley
8. Linux Device Drivers, 2nd Edition, By Alessandro Rubini & Jonathan Corbet, O'Reilly
9. Embedded Systems Architecture Programming and Design: 1st Edition; by: Raj Kamal, Tata McGraw Hill

In addition, National/ International journals in the field, data sheets, application notes and research papers in journals are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

Annexure – 1

Linux Assignment # 1

File Management

1. Write a program to create a file and set different permissions and check the user permissions by using system call from another program also print the error message. [Hint: use access(), perror() system calls]
2. Write a program, which creates a file of given name and writes a string to the given file.? [Hint: fopen(), fclose(), fputc() library function calls]
3. Write a program, which read contents of above created file and display it on the screen? [Hint: open(), read() , write(), close syatem calls]
4. Write a program, which creates file with given name and writes the byte values from 0 to 0xff. The program closes the file and returns. Now try to open the file created in the above step, using the vi editor. What do you expect to see? [Hint: fopen(), fclose(), fprintf() library function calls]
5. Write a program, which creates a file of given name and writes a variable length string entered to the given file. ? [Hint: fopen(), fclose(), fdopen(), fgets() library function calls use ctrl+D to quit writing]
6. Write a program to write a given structure to a new file in ASCII format.

   ```
   typedef struct
   {
   char name[30];
   int account;
   int balance;
   };
   ```

   Collect data from the user and initialize the structure (at least 5 structures).Write the data to the given file. Close the program and view using vi editor.

Process Management

1. Write a program to get and print the following process identifiers. Process Id, parent process id, user id, group id .
2. Run the following program.

   ```
   Main ( )
   {
     printf ("I am forking a child process\n");
     fork ( ) ;
     printf ("who am I ? child or parent ? My Id process : %u \ n",
             getpid ( ) );
   }
   ```

3. Rewrite the above program, which identifies the process as parent or child based on the return value of fork ( ) and displays all the process identifiers given problem 2.
4. Write a program in which parent forks a child process. Parent displays a message saying that he is going to wait for the termination of child process. Next parent calls

the wait ( ) function. The child process implements a while (1) loop. In this loop it reads a string from standard input. Compare the string with “exit”. If it matches, child terminates using exit ( ) call. For any other string it simply displays the string.

5. Write an “hello world\n” program. Write a separate program, which runs the hello World program using ‘execv’ system call.
6. Write a Linux shell program, which accepts basic command from user. [Hint: basic command path /bin/ and exec system call]

I/O Management

1. Write a program to open the serial port device on the Unix/Linux machine. Take data from the user and send the data over a serial channel.
2. Write a program to open the serial port device read the data from the device and Display data received from the serial port.
3. Open the serial device and get the control parameters of serial device and display them.
4. Modify the program 1 and 2 to take the baud rate from the user and to set the Device to the baud rate using the device.
5. Combine the functionality of program 1 and 2 into a single program by forking Additional process. The parent process should take the data from the keyboard and should send that data to the serial device. The child process should read data from the serial port and display the received data on the console.
6. Implement the functionality of problem 5, with a single process by using the Select functionality.

Thread Management

1. Write a program to create a thread that displays a string and terminates the thread.
2. Write a program to create threads (at least three) which displays the thread identifier for the thread being created. Implement such that threads waits for it to finish using the **pthread_join** function. Once the threads have finished executing display the number of threads created.
3. Write a program to create a child thread which calculates the square of a number. Receive the result in the parent thread and display the output. Use **pthread_join** function with status.
4. Write a program to create threads (at least three) which increments a variable counter 'n' number of times. Display the value of variable once the threads have finished executing. Run the program with different values of ‘n’ and notice the output.
5. Modify the above program with mutex, for protecting the variable ‘n’ from multiple accesses by the threads. Check the output.
6. Write a program to create a producer thread that creates work and N consumer threads that operate on the work using condition variables. The producer thread creates work, increments a counter and awakes all threads waiting the condition. The consumer thread decrements the counter and wait until the work has been finished. Display the consumer thread id once it starts working.

Annexure – 2

Inter Process Communication Assignment # 1

Pipes and FIFO's

1. Write a program to create a pipe within a process, write a message to the pipe and read the message back from the pipe and display it.

2. Write a program which fork a child process with command 'ls –l' and parent process with command 'wc –l'. Create a pipe between parent and child. Dup the write end of child process to stdout and read end of parent process to stdin.

3. Create a fifo using mkfifo command from the command line and set its permissions (full). Try to read the fifo using the cat command. Now open another terminal and write a string to fifo using cat command. View the output on the other terminal.

IPC with Semaphores

System V semaphores:

1. Write a program to create a semaphore with **semget** function. Write another program which tries to acquire the semaphore created. Run this program in the background. It will be in the wait state not able to acquire the semaphore. Now write a separate program which releases the semaphore,such that second program will be able to acquire the semaphore.

2. Write a program to set the current semaphore count. Write a separate program to read the semaphore count.

3. Write a program to create a semaphore array of 5 semaphores. Set the values of semaphore array using SETALL command. Read the values assigned using GETALL command.

4. Write a program to create a semaphore and read the following information of semaphores. Last semop time, Last change time, owner user ID, owner group ID, Creator user ID, Creator group ID, mode of permission.

5. Modify program 1 with array of semaphores.

Posix Semaphores:

1. Write a program to fork a child process and create a semaphore. Initialize a shared variable. The child process should increment the shared variable and parent process should decrement the variable. Protect the variable using semaphores and get the value of semaphore using sem_getvalue function.

   (Use sem_open to create the semaphore. Use sem_wait and sem_post function to protect the variable.)

2. Write a program to create two threads which increments a variable counter 'n' number of times. Display the value of variable once the threads have finished executing. Use

semaphores to protect the variable from multiple access. Check the output.
(run program as gcc 1.c -o 1.exe -lrt)

Shared Memory

System Shared Memory

1. Write a program to create a shared memory segment, write a string to it and read from the segment.

2. Write a program to create a shared memory and retrieve the following information about the shared memory segment. Segment size, Last change time, PID of segment creator, PID of last segment user, Number of current attaches, permission mode.

3. Write a program to print the access permission of a shared memory segment created and change the permission.

4. Implement a client server process as two separate programs communicating through shared memory.
5. The server program should create a shared memory and write a string to the shared memory segment. The client program should attach itself to the shared memory and read from it.

6. Write a program to create a shared memory segment. Give the arguments from the command line. Write some data to the shared memory, protect the critical section using semaphores. Read data from the shared memory and display it.

Posix Shared Memory

1. Write a program to create a shared memory segment. Set the length of the segment and map the object into the address space of the process. Write a set of numbers to the shared memory segment.
2. Write a program to read the numbers written to the shared memory segment.
3. Write a server program that creates a shared memory segment, initializes the semaphore and then terminates. Pass the arguments from the command line. Write a client program that increments the counter in the shared memory some 'n' number of times. Protect the variable using semaphore. Run the client program multiple times such that the counter variable will be accessed by many programs at a time. (include -lrt)

Annexure – 3

VxWORKS Assignment #1

Scheduling and Task Management:

1: Create task1 with some priority. Now from task1 create other task (task2). Now that task2 sleeps for some time(100ms).Observe the execution sequence by looking at the 'printf' statements.

2: Repeat the above by disabling the pre-emption.

3: Create two tasks with different priorities. Task1 should delay for 5 sec and then task2 should delay for 10 sec continuously. Observe the sequence of execution of the task.

4: Create task1 with highest priority .Now from task1 create two other tasks with different priorities. Observe the sequence of execution of the tasks. Now change the task priorities alternatively (do all possible priorities for the 3 tasks) and observe the sequence of execution of the tasks.

5: Create deadlock condition by creating the tasks with different priorities (low, middle, high) and resolve it by using priority inheritance.

6: Create 3 tasks with different priorities and let lower priority task run continuously by disabling preemption and protect the lower priority task from unexpected deletions.

7: Write a root fun which creates fixed length msg queues. create task1, task2.write task1,which sends a msg to msg queue and task2 receives it and prints. Interchange the priorities and observe. Repeat the above with different msg queue lengths.

8: Write a root fun creates task1, task2, task3 & task4. Task1 should send a msg to the msg queue created by the root fun. Task2,3,4 -should receive it and print.

9: Write a root fun which creates a task and sets VxWorks time to a known value; get VxWorks time and print it.Make task to sleep for 5 secs and get the VxWorks time and print it.

10: Create task1 with priority 20 and task2 with priority 10.execute task1 1 sec and task2 every 1/2 sec .if "a" is printed from task1 and "b" is printed from task2. Observe the sequence of execution.

11: Data Display task.
The root task creates the display task and root task suspends itself.

This task draws the meters for a set of parameters on the screen initially. Next it periodically updates the value of parameters in the meter. Each parameter is available as a global variable. The task reads and displays this variable on the corresponding meter.

This display task sleeps for one second and again updates the values on the meters. This task repeats the same thing in a forever loop. While this task is running all the parameters remain constant.

12: Data simulator task

Root task creates both the display task and simulator task.

This task also periodically wakes up from the sleep and increments the global parameter value. If the value reaches the maximum, it resets it to the minimum value. Make data simulator task to run once in every 100 milliseconds (that mans it should sleep for 100 milliseconds).

Now the data being displayed by display task should continuously get changed.

13: Multiple data simulator tasks

The root task creates display task and multiple simulator tasks.

Instead of a single simulator task, create multiple simulator (4) tasks. Each task sleeps for different amount of time (100ms,50ms,1 sec,2 sec). Each task updates (incrementing) only a set of parameters. Once this program is running some parameters should change more rapidly than the other parameters.

I/O Systems:

14: Mutual exclusion of simulator task and display task using semaphore.

Semaphores are used for task synchronization and also for mutual exclusion or resource sharing. Now let us use semaphore for mutual exclusion.
Let us assume simulate tasks are of higher priority than display task. Here simulator task is a kind of input task, which is responsible for reading the input data like analog inputs and digital inputs. So one should read the input values periodically, that's why we made input (simulator) tasks of higher priority than display task.

But one requirement is that, while display task is displaying the parameters, no simulator task should change the parameters in between. Basically we want to display parameters, which are completely updated ones or old ones. We do not want some parameters to be of latest ones and others are old ones.

Create a semaphore with a token value of 1. Display task acquires this semaphore and display all the parameters and releases the semaphore. Same way each simulator task also acquires this semaphore, updates the parameters and releases the semaphore.

Note: use the exercise 3 of assignment 1 as the base code for this program

15**:** Synchronizing display task and simulator tasks with a semaphore.

So far display task and simulator tasks are running independently (ie. Asynchronously). So some timid may happen that display task will update even when no input (simulator is our input) task is updated the values. So let us synchronize. Create a semaphore with no tokens. Each simulator task will send a token to semaphore whenever it updates the parameters. The

display task always waits at the semaphore and whenever it gets a token it displays all the parameters.

Note1: Use the exercise 3 of assignment 1 as the base code for this program.
Note2: Now display task will never goes to sleep and always waits on semaphore.

16**:** Inter process communication between simulator task and display task using message queues and partition buffers.

In this program let us have one display task and one simulator task. The root task creates display task simulator task and a message queue.

Simulator task runs periodically (say once in every 200 milliseconds) whenever it runs it stimulates all the parameters (increment and reset once reaches maximum value) next it forms the message and send the messages to the message queue. The first integer in the message contains the number of parameters present in the message each parameter contains two values first one is parameter id and second one is its value. This is format of the message.

The display task waiting at the message queue receives the message. The display task displays the parameters in the message.

17**:** Extend the above program by having two simulator tasks. Each simulator task sends a separate set of parameters to the message queue.

18**:** Redo the above experiment by using pipes instead of using message queues.

Annexure – 4

RT Linux Assignment # 1

1: Write a program to print "welcome to RT-Linux" in RT-Linux environment.

2: Write a program to create a thread which displays the argument passed from thread creation also try to create another thread from the exciting thread also set stack before creation of new thread.
[Use rtl_gpos_malloc (32768), pthread_attr_setstacksize (), pthread_attr_setstackaddr () API's]

3: Repeat the above program also print the stack size by using API's from the thread2. [Use rtl_gpos_malloc (32768), pthread_attr_setstacksize (), pthread_attr_setstackaddr (), get_stacksize () API's]

4: Write a program to create a thread1 which allocate stack size for new thread and create another thread, thread2 which calculate the square of a number and pass the result as return value to thread1.And main thread should be in waiting until thread1 finishes its execution.
[Use rtl_gpos_malloc (32768), pthread_attr_setstacksize (), pthread_attr_setstackaddr () API's]

5: Write a program to create a thread which displays the seconds by using printf statement. [Use clock_gettime (), timespec_add_ns (), clock_nanosleep () API's]

6: Write RTLinux program to create three threads. Every thread does the same thing (function thread_code), but different string parameters are passed to each of them. (Passing string parameter is "This is thread x" (x=1 or 2 or 3))

O/p of the program should be in the following form and

From thread1 (in between Each printf one second delay should be there)

Message: This is thread 1

Message: This is thread 1

Message: This is thread 1

Thread 1 has stared

From thread2 (in between Each printf one second delay should be there)

Message: This is thread 2

Message: This is thread 2

Message: This is thread 2

Thread 2 has started

From thread3 (in between Each printf one second delay should be there)

Message: This is thread 3

Message: This is thread 3

Message: This is thread 3

Thread 3 has started

7: Modify the above program with out altering rtl_printf () statements should print the following at the statement on the shell

Thread 1 has started

Thread 2 has started

Thread 3 has started

Message: This is thread 1

Message: This is thread 3

Message: This is thread 3

Message: This is thread 3

Message: This is thread 2

Message: This is thread 2

Message: This is thread 2

Message: This is thread 1

Message: This is thread 1

8: Create thread1 with some priority. Now from thread1 create other thread (thread2). Now that thread sleeps for some time. Observe the execution sequence by looking at the 'printf' statements.

[Hint: can use thread_setschedparam (), pthread_make_periodic_np (), pthread_wait_np () APIs]

9: Create thread1 with highest priority .Now from thread1 create two other threads with different priorities. Observe the sequence of execution of the threads. Now change the thread priorities alternatively (do all possible priorities for the 3 threads) and observe the sequence of execution of the threads.

10: Write a program to create initially an empty binary semaphore, and also crate thread1, which is waiting to get the semaphore for its further completion and create another thread (thread2) which posts the semaphore. See the working by using printf statements.

11: Write a program to create three threads [withdraw, deposit, query] which access simultaneously to the bank account (created at the main thread). Deposit thread deposits Rs 5000/- (as one by one), Withdraw thread withdraws Rs350/-(one by one) and query thread check the balance at the same time. Observe the query result and final balance (after finishing threads).

12: Repeat the above program with mutex semaphore as a protection to the bank account while doing any of three transactions (deposit, query, withdraw).Compare the output of this program with the previous result.

13: Write a program to create a square wave by using parallel port interrupt method.

Run the program by using normal Linux environment. Run any delay program parallel with the wave generation program. See the effect of wave form after the parallel execution.

14: Repeat the above example with the wave form generation as an RT-thread and note down the effects.

THIRD SEMESTER

EDT 15 301 - ELECTIVE IV
&
EDT 15 302 - ELECTIVE V

A - WIRELESS TECHNOLOGIES

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 - RF Basics: **Radio Frequency (RF) Fundamentals:** Introduction to RF & Wireless Communications Systems, RF and Microwave Spectral Analysis, Communication Standards, Understanding RF & Microwave Specifications. Spectrum Analysis of RF Environment, Protocol Analysis of RF Environment, Units of RF measurements, Factors affecting network range and speed, Environment, Line-of-sight, Interference, Defining differences between physical layers- OFDM, HR/DSSS,MIMO **Spread Spectrum Concepts:** OFDM & HR/DSSS channels, Co-location of HR/DSSS and OFDM systems, Adjacent-channel and co-channel interference, WLAN / WPAN co-existence, CSMA/CA operations **RF Antenna Concepts:** Passive gain, Beam widths, Simple diversity, Polarization, Antenna Mounting, Wireless Antennas and Accessories, RF cables, RF connectors, Lightning arrestors and grounding rods	8
Module 2 – Cellular Standards Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells, Handoff, 1^{st}, 2^{nd}, 3^{rd} and 4^{th} Generation Cellular Systems (GSM, CDMA,IS-95, GPRS, EDGE,UMTS, EVDO, CDMA2000), Mobile IP, WCDMA	11

Module 3 – WLAN **Wi-Fi Organizations and Standards:** Regulatory Bodies, IEEE, Wi-Fi Alliance, WLAN Connectivity, WLAN QoS & Power-Save, IEEE 802.11 Standards,802.11-2007,802.11a/b/g, 802.11e/h/I,802.11n **Wi-Fi Hardware & Software:** Access Points, WLAN Routers, WLAN Bridges, WLAN Repeaters, WLAN Controllers/Switches, Direct-connect Aps, Distributed-connect Aps, PoE Infrastructure, Midspan, Endpoint, Client hardware and software, Antenna types and uses Wi-Fi Security concepts, Wi-Fi Applications	11
Module 4 – WSN & WPN Wireless Personal Area Networks, Bluetooth, Bluetooth Standards, BlueTooth Protocol Architecture,UWB, IEEE 802.15 standards, ZigBee, Sub1GHz, Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks, Routing protocols in Wireless Sensor Networks.	9
Total Hours	**39**

TEXT BOOKS:

1. Wireless Communications – Principles and Practice; by Theodore S Rappaport, Pearson Education Pte. Ltd., Delhi
2. Wireless Communications and Networking; By: Stallings, William; Pearson Education Pte. Ltd., Delhi
3. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi
4. Wilson , "Sensor Technology hand book," Elsevier publications 2005.
5. Andrea Goldsmith, "Wireless Communications," Cambridge University Press, 2005

REFERENCES:

1. Mobile and Personal Communications Services and Systems; 1st Edition; By: Raj Pandya; PHI, New Delhi
2. Fundamentals of Wireless Communication by Tse David and Viswanath Pramod, Cambridge University press, Cambridge
3. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi
4. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi

6. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi
7. Holger Karl and Andreas Wiilig, “Protocols and Architectures for Wireless Sensor Networks” John Wiley & Sons Limited 2008.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	**Module 2**	**Module 3**	**Module 4**
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

B - AUTOMOTIVE ELECTRONICS

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 Automotive fundamentals: Automotive physical configuration, Engine, ignition system, drive train, suspension, brakes, steering system. Systems approach to control and instrumentation: Characteristics of digital electronic system, Instruments, Control system.	7
Module 2 Basics of Electronic Engine control: Motivation for electronic engine control, concept of an electronic engine control, definition of engine performance terms, Engine Mapping, control strategy, electronic fuel control system, electronic ignition. Sensors and actuators: Air flow rate sensor, engine crank shaft angular position sensor, throttles angle sensor, temperature sensor, oxygen sensor, knock sensor. Automotive engine control actuators.	12
Module 3 Digital Engine control system: Digital Engine control features, control modes for fuel control, EGR control, Electronic ignition control, integrated engine control system.	10
Module 4 Vehicle motion control: Cruise control system, Antilock braking system, Electronic suspension system, Electronic steering control, automotive instrumentation, on board and off – board diagnostics, occupant protection systems.	10
Total Hours	**39**

TEXT BOOK

1. William B. Ribbens " Understanding Automotive Electronics" 6th Edition, Newnes

REFERENCE

1. Betchtold., " Understanding Automotive Electronics" SAE, 1998

In addition, relevant papers in journals & articles etc. are to be referred to get further information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

C - MIXED SIGNAL SYSTEM DESIGN

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 Introduction PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing, Example of Analog Mixed Signal Circuit Design	8
Module 2 Digital Sub Circuits CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders. Digital Circuits like ALU, Comparator, Parity generator, Timer, PWM,SRAM and DRAM,CAM	10
Module 3 Analog Sub circuits Ideal Operational Amplifier, Inverting and Non-inverting configuration Differential amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier	10
Module 4 Data Converters **DAC** : Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs **ADC** : Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit ,Quantization error, Concept of over sampling, Counting ADC, Tracking ADC, Successive approximation ADC, Flash ADC, Dual Slope ADC **Over sampling Data Converters** : Over sampling fundamentals, Delta –Sigma Converter basics, $\Delta \sum$ Modulator	11
Total Hours	**39**

TEXT BOOKS:

1. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition
2. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley
3. Ken Martin, Digital Integrated Circuit Design, John Wiley
4. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3rd edition, John Wiley & Sons.
5. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)
6. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits – A Design Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition).
7. Sung-Mo Kang**,** Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design,2nd Ed, Tata McGraw Hill

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

D - ROBOTICS AND MACHINE VISION

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 - Industrial Robots: Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations, Industrial Applications of Robots, and Programming	12
Module 2 - Introduction Machine Vision: Principles of Machine Vision, Vision and factory automation, Human Vision Vs. Machine Vision, Economic Considerations, Machine Vision – System Overview, Image acquisition – Illumination, Image formation and Focusing, Image Detection – Introduction, Types of Cameras; Image Processing and Presentation.	8
Module 3 - Image Processing Techniques and Transformations: Fundamental Concepts of Image Processing, Pixel, Pixel Location. Gray Scale, Quantizing Error and Measurement Error and Histograms. Basic Machine Vision Processing Operators – Monadic one Point Transformations: Identity operator, Inverse Operator, Threshold operator and other operators viz: Inverted Threshold operator, Binary Threshold operator, Inverted Binary Threshold Operator, Gray Scale Threshold and Inverted Gray Scale Threshold Operators; Dyadic Two Point Transformations – Image Addition, Image Subtracting, Image Multiplication; Convolution and Spacial Transformations	10
Module 4 - Edge Enhancement Techniques and Image Analysis: Introduction, Digital Filters – Low pass and High Pass filters; Edge Engancement Operators – Laplacian, Roberts Gradient, Sobel and other Local operators. Image Analysis: Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm.	9
Total Hours	**39**

TEXT BOOKS:

1. Machine Vision and Digital Image Processing, by Louis J. Galbiati, Jr. Prentice Hall, Englewood Cliffs, New Jersy.`
2. Robotics for Engineers, By, Yoram Koren, McGraw Hill.
3. Robotics and Image Processing – an Introduction, by Janakiraman P. A., Tata McGraw Hill, New Delhi

4. Digital Image Processing and Computer Vision by Robert J.Schalkoff, John Wiley & Sons Inc.

REFERENCES:

1. Industrial Robotics – Technology, Programming and Applications, by Mikell P. Groover, Mitchell Wein, Roger N. Nagel and Nicholas G. Odlrey, McGraw Hill International Edistion.
2. Handbook Of Image Processing Operators by Klette, Reinhard & Zamperoni, Piero; John Wiley & Sons Inc
3. Image Processing, Analysis And Machine Vision by Sonka, Milan Et Al
4. Industrial Robotics by Hodges, Bernard, Jaico Publishing House, Delhi
5. Introductory Computer Visiona dn Image Processing by Adrian Low, McGraw Hill International Editions.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

E - ELECTRONIC INSTRUMENTATION DESIGN

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1 Architecture of Instrumentation scheme. Static and dynamic characteristics, errors, standards and calibration. Principle and design of various active and passive transducers. Introduction to semiconductor sensors and its applications. Electrical I/O characteristics of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion. Specifications and selection of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion.	8
Module 2 Amplification, attenuation, isolation, multiplexing, filtering, linearization, compensation, simultaneous sampling & transducer excitation. Operational and Instrumentation Amplifiers. Instrumentation amplifiers and Error Budgets, Noise in low level Amplification.	10
Module 3 Analog Signal Acquisition, Conditioning and Processing, Input grounding, Shielding and Termination Practice. Signal conditioning Error Analysis. DC, Sinusoidal and Harmonic Signal Conditioning, Analog Signal Processing, Devices for Data Conversion – Analog Multiplexers, Sample – Holds, D/A and A/D Sampled Data, Inter sample Error and Interpolation, Aliasing of Signal and Noise, Inter sample and Aperture Error, Signal Recovery and Interpolation Conversion System Design with Computer – Assisted Analysis, System Design Considerations, Computer Assisted Interface Analysis Software	12
Module 4 Introduction to smart sensors, Voltage to Frequency Converters and Frequency to Code converters, Data Acquisition methods for multi Channel sensor systems, Smart sensor design, Smart sensor Buses and Interface circuits.	9
Total Hours	**39**

TEXT BOOKS

1. Measurement and Instrumentation Principles, by: Alan S. Morris, Butterworth-Heinemann
2. Advanced Instrumentation and Computer I/O Design, by: Patrick H. Garrett, IEEE Press
3. Data Acquisition and Signal Processing for Smart Sensors, by: Nikolay V. Kirianaki et al., John Wiley & Sons
4. Microsensors MEMS and Smart Devices, by: Julian W. Gardner, Vijay K. Varadan, et al., John Wiley & Sons

REFERENCES

1. Industrial Instrumentation Principles and Design, 1st edition; by:Tattamangalam. R.Padmanabhan, Springer Verlag.
2. Measurement Systems Application and Design, by: Ernest O. Doebelin, McGraw-Hill Science/Engineering/Math
3. Handbook of Transducers, 1st edition; by: Harry N.Norton, Prentice Hall.
4. Advances in Distributed Sensor Technology; by: S.S.Iyengar, L.Prasad, Hla Min; Prentice Hall PTR
5. Standard Recommended Practises for Instrumentation & Control, Vol 1-3,11th edition; Instrument Society of America.
6. Microsensors: Principles and Applications; by: Gardner, J W, Wiley (1994)
7. Measurement Systems, Application and Design, 4th edition; by: Ernest O.Doebelin, McGraw- Hill.
8. Practical Design Techniques For Sensor Signal Conditioning; Seminar Materials@ http://www.analog.com
9. Data Acquisition Fundamentals; Application Note AN007 @ http://www.ni.com
10. Measurement Systems And Sensors (Hardcover), By: Waldemar Nawrocki , Artech House Publishers
11. Introduction to Instrumentation and Measurements, by: Robert B. Northrop, CRC; 2 edition
12. Microtransducer CAD: Physical and Computational Aspects (Computational Microelectronics) (Hardcover), by: Arokia Nathan (Author), Henry Baltes (Author), Springer

In addition National & International journals in the related topics shall be referred. Manufacturer's device data sheets and application notes are to be referred to get practical application oriented information.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

F - ADVANCED DIGITAL COMMUNICATION

Maximum Marks – 100; Credits - 3

Topics	Hours
Module 1: Digital communication system (description of different modules of the block diagram), Complex baseband representation of signals, Gram-Schmidt orthogonalization procedure. M-ary orthogonal signals, bi-orthogonal signals, simplex signal waveforms. Pulse amplitude modulation (binary and M-ary, QAM), Pulse position modulation (binary and M-ary), Carrier modulation (M-ary ASK, PSK, FSK, DPSK), Continuous phase modulation (QPSK and variants, MSK, GMSK).	10
Module 2: Coherent and non-coherent demodulation: Matched filter, Correlator demodulator, square-law, and envelope detection; Detector: Optimum rule for ML and MAP detection Performance: Bit-error-rate, symbol error rate for coherent and non-coherent schemes.	9
Module 3: Pulse shape design for channels with ISI: Nyquist pulse, Partial response signaling (duo binary and modified duo binary pulses), demodulation; Channel with distortion: Design of transmitting and receiving filters for a known channel and for time varying channel (equalization); Performance: Symbol by symbol detection and BER, symbol and sequence detection, Viterbi algorithm.	10
Module 4 Different synchronization techniques (Early-Late Gate, MMSE, ML and spectral line methods). Characteristics of fading channels, Rayleigh and Rician channels, receiver performance-average SNR, outage probability, amount of fading and average bit/symbol error rate.	10
Total Hours	**39**

TEXTBOOKS:

1. J. G. Proakis and M. Salehi, Fundamentals of Communication Systems, Pearson Education, 2005.
2. S. Haykins, Communication Systems, 5th ed., John wiley, 2008.
3. M. K. Simon, S. M. Hinedi and W. C. Lindsey, Digital Communication Techniques: Signaling and detection, Prentice Hall India, N. Delhi, 1995.
4. W. Tomasi, Advanced Electronic Communication Systems, 4th Ed., Pearson Education, 1998.
5. M. K. Simon and M. S. Alouini, Digital Communication over Fading Channels, 2000.

REFERENCES:

1. Simon Haykin,Digital Communications , 2006, John Wiley & Sons.
2. B.P. Lathi,Modern Digital and Analog Communication, 3rd Ed., Oxford UniversityPress.
3. Sklar, Digital Communication, 2E, Pearson Education.
4. K.Sam Shanmugham,Digital and Analog Communication Systems, John Wiley &Sons
5. R.E. Ziemer and W.H. Tranter,Principles of Communications, JAICO PublishingHouse.
6. H.Taub and Schilling,Principles of Communication Systems, TMH
7. Pierre Lafrance,John G.Proakis,Digital Communications, McGraw Hill.
8. Couch, Analog and Digital Communication.5th Ed,PHI

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

G - VLSI SIGNAL PROCESSING

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Graphical representation of DSP algorithms, Dataflow and control flow. Introduction to Pipelining and Parallel Processing, Parallel pipelined design of DSP Algorithms. Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques. Unfolding Introduction, An algorithms for unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding. Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures	10
Module 2: Design of VLSI Architectures for Digital Signal Processing: Architectural Design at Register Transfer Level, Design of Data path elements, Control structures, Testable and self-reconfigurable fault-tolerant structures. Speed-Area-Power tradeoff issues related to mixed signal design and SoC.	9
Module 3: Filter structures, Transform structures, Data Flow and Control flow issues. Array processing approaches to DSP solutions. Introduction to spatial filters. Development of VLSI architecture for spatial filter.	10
Module 4: Modern DSP algorithms (Audio, Video and Multimedia) and development of new computational and arithmetic building blocks. VLSI Architecture development for JPEG2000 video CODEC and performance comparisons.	10
Total Hours	**39**

TEXT BOOKS:

1. VLSI Signal Processing Systems - Keshab K Parhi, John Wiley and Son's, NY 1999.
2. Architectures for Digital Signal Processing - Peter Prissch, John Wiley and Son's NY 1998.
3. Introduction to Data Compression, 2nd Edition - Khalid Sayood, Harcourt India, New Delhi, 2000.

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

H - CLOUD COMPUTING

Maximum Marks – 100; Credits - 3

Modules	Hours
Module 1: Cloud Computing – History of Cloud Computing – Cloud Architecture – Cloud Storage – Why Cloud Computing Matters – Advantages of Cloud Computing – Disadvantages of Cloud Computing – Companies in the Cloud Today – Cloud Services Web-Based Application – Pros and Cons of Cloud Service Development – Types of Cloud Service Development – Software as a Service – Platform as a Service – Web Services – On-Demand Computing – Discovering Cloud Services Development Services and Tools – Amazon Ec2 – Google App Engine – IBM Clouds.	10
MODULE 2: Centralizing Email Communications – Collaborating on Schedules – Collaborating on To-Do Lists – Collaborating Contact Lists – Cloud Computing for the Community – Collaborating on Group Projects and Events – Cloud Computing for the Corporation.	10
MODULE 3: Collaborating on Calendars, Schedules and Task Management – Exploring Online Scheduling Applications – Exploring Online Planning and Task Management – Collaborating on Event Management – Collaborating on Contact Management – Collaborating on Project Management – Collaborating on Word Processing - Collaborating on Databases – Storing and Sharing Files.	10
MODULE 4: Collaborating via Web-Based Communication Tools – Evaluating Web Mail Services – Evaluating Web Conference Tools – Collaborating via Social Networks and Groupware – Collaborating via Blogs and Wikis.	9
Total Hours	**39**

TEXT BOOKS:

1. Michael Miller, Cloud Computing: Web-Based Applications That Change the Way You Work and Collaborate Online, Que Publishing, 2008.

REFERENCES:

1. Dan C. Marinescu , Cloud computing: Theory and Practice, Morgan Kaufmann, 2013
2. Kai Hwang, Geoffrey C. Fox, Jack J. Dongarra, Distributed and Cloud Computing,: From Parallel Processing to the Internet of Things, 1/e, Morgan Kaufmann , 2011

Internal Continuous Assessment: 50 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

End Semester Examination: 50 marks

Question Pattern

Answer any 5 questions by choosing at least one question from each module.

Module 1	Module 2	Module 3	Module 4
Question 1 : 10 marks	Question 3 : 10 marks	Question 5 : 10 marks	Question 7 : 10 marks
Question 2 : 10 marks	Question 4 : 10 marks	Question 6 : 10 marks	Question 8 : 10 marks

EDT 15 303 SEMINAR

SEMINAR	Maximum Marks – 100; Hours/week: 2	Credits: 2

	Hours
Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.	Per week 2
Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 15 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.	
Internal continuous assessment: 100 marks	

Subject Relevance	:	10 marks
Concept/ Knowledge in the topic	:	20 marks
Presentation	:	40 marks
Report	:	30 marks
Total marks	:	**100 marks**

EDT 15 304	MASTER RESEARCH PROJECT PHASE I Maximum Marks – 50; Hours/week: 16	Credits: 6

Objective:

To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute, subject to the conditions of M.Tech regulations. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee shall be headed by the head of the department with two other faculty members in the area of the project, of which one shall be the project supervisor..

For this a committee

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

Internal Continuous assessment: 50 Marks

	Supervisor/ Guide	Evaluation Committee
Project Review	**20 Marks**	**30 Marks**

FOURTH SEMESTER

EDT 15 401	MASTERS RESEARCH PROJECT PHASE II Maximum Marks – 100; Hours/week: 24	Credits: 12

Objective:

To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

Master Research project phase II is a continuation of project phase I started in the third semester. There would be two reviews in the fourth semester, first in the middle of the semester and the second at the end of the semester. First review is to evaluate the progress of the work, presentation and discussion. Second review would be a pre-submission presentation before the evaluation committee to assess the quality and quantum of the work done. This would be a pre qualifying exercise for the students for getting approval by the departmental committee for the submission of the thesis. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation. This shall be done by a committee constituted for the purpose by the principal of the college. The concerned head of the department shall be the chairman of this committee. It shall have two senior faculty members from the same department, project supervisor and the external supervisor, if any, of the student and an external expert either from an academic/R&D organization or from Industry as members.

Internal Continuous assessment: 100 Marks

	Supervisor/ Guide	External Expert	Evaluation Committee
Project Review	**30 Marks**	**30 Marks**	**40 Marks**