QUALIFICATION FILE TEMPLATE

NSDA REFERENCE To be added by NSDA

QUALIFICATION FILE – CONTACT DETAILS OF SUBMITTING BODY

Name and address of submitting body: NIELIT J&K 1.SIDCO Electronics Complex, Rengreth, Srinagar-191132 2.New Campus, University Of Jammu, Jammu-180006 3.Council secretariat Leh. Name and contact details of individual dealing with the submission Name Shri DS Oberoi/ Shri Ravi Rastogi Position in the organisation Scientist-E/Scientist-C Address if different from above NA Tel number(s) 0191-2455515,2455514,2432291 **E-mail address** oberoi@nielit.gov.in, ravirastogi@nielit.gov.in CC To dir-srinagar@nielit.gov.in

List of documents submitted in support of the Qualifications File

- 1. Industry Validation (Annexure I)
- 2. Detailed Curriculum (Annexure II)

SUMMARY

Qualification Title:	Post Diploma in VLSI Design,
	Tools and Technology
Qualification Code	NL/M/L5/C017
	NIELIT/EM/L5/013
Nature and purpose of the qualification:	 Nature: Post Graduate Diploma Course which will help in Employment in the area of VLSI and Embedded System. Purpose: To Provide Employment in Electronic Circuit Designing, Testing Industries. To upgrade the skills of incumbent working in field of Analog, Digital & Mixed VLSI Integrated circuits, Entrepreneurship Development.
Body /bodies which will award the qualification:	Examination Cell National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Body which will accredit providers to offer courses leading to the qualification:	National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Body /bodies which will Be responsible for assessment:	National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Occupation(s) to which the qualification gives access:	Layout Engineer, Circuit Test Engineer, VLSI CAD Designer
Licensing Requirements	N/A
Proposed level of the qualification in the NSQF	Level 5
Anticipated volume of training/learning required to complete the qualification	400 Hours
Entry requirements Recommendations	Diploma Holder, B Sc. Graduate
Progression from the Qualification	Academic Higher level course in relevant field ->B tech in

	VLSI/Electronic system design-> M Tech in VLSI
	This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by Embedded & VLSI markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices.
	Professional
	This uniquely hybrid course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries like:
	a. Circuit Layout Designingb. Circuit Testingc. Research and Development
	For people interested in entrepreneurships this would be an excellent launch pad. In addition the course also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.
Planned arrangements for RPL.	The candidates who will undergo such training shall be accessed through written test, viva-voce to evaluate the candidate's aptitude for the course
International Compatibility where Known.	No
Date of Planned review of the Qualification	After Every 2 Years

Format Structure of the Qualification			
Title of Component and Identification Code	Mandatory/ Optional	Estimated Size (Learning hours)	Level
INTRODUCTION VLSI Design Flow and Y-Chart, Front-Back End VLSI Design and Verilog and Simple Logic Gates Coding,	М	25	5
Programmable Logic Devices (PLDs) Introduction, PLDs Types-Simple PLDs (SPLDs), Complex PLDs (CPLDs) and Field Programmable Gate Array (FPGA),	М	35	5
System Verilog Code Structure and FPGAImplementationModule Declaration Analog Block Statements, Mathematical Functions.	М	100	5
VLSI Technology Basic MOS Transistor Operations and Electrical Properties, Fabrication Process, Development in Technology.	М	40	5
VLSI Design- Part 1 VLSI Design Style, CMOS Fabrication and Electrical Properties, Dynamic, Clocked, Domino CMOS Logic VLSI Design Style,	М	40	5
SPICE Modeling for VLSI Design-Part 2 SPICE Tutorials and Commands, Sources and Passive Components, CMOS Inverter Transient Analysis,	М	100	5
File Interchange Format for VLSI Design Need for File Inter Change,	М	30	5
Design Verification Functional and Test Bench Verification using System, Verification Methodology-OVM, UVM, AVM and ABV Verilog,	М	30	5

Please attach any document giving further detail about the structure of the qualification-e.g. a Curriculum or Qualification Pack. Detail Curriculum attached at **Annexure II.**

SECTION -1

ASSESSMENT

Name of Assessment body:

Examination Cell, National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.

Name of body checking or verifying Assessments: Examination Cell, National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi, 110003.

Name of Qualification Awarding body:

National Institute of Electronics and Information Technology.

Will the assessment body be responsible for the RPL assessment?

Give details of how RPL assessment for the qualification will be carried out and quality assured.

The candidates who undergo such training shall be accessed through written, viva and project. Later on, candidate can appear for similar or advanced level of certification course if they fulfil entry requirements there.

Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of NSQF:

The emphasis is on theory as well as on practical & knowledge based on the performance criteria. Student is required to pass in all evaluations individually and marks will be allotted.

The Following assessment methodologies are used.

- A. Written Assessment.
- B. Practical Assessment & class Performance.
- C. Viva-Voce.
- D. Project.

The assessment results are backed by following evidences.

1. The assessor collects a copy of the attendance for the training done under the scheme. The attendance sheets are signed and stamped by the In-charge / Head of the Training Centre.

- 2. The assessor verifies the authenticity of the candidate by checking the photo ID card issued by the institute as well as any one Photo ID card issued by the Central/Government. The same is mentioned in the attendance sheet.
- 3. The assessor assigns roll number.
- 4. The assessor takes photograph of all the students along with the assessor standing in the middle and with the centre name/banner at the back as evidence.

Please attach any documents giving further information about assessment and /or RPL.

ASSESSMENT EVIDENCE

Job Role

- Circuit Layout Designing and Testing Engineer.
- VLSI and Embedded Programmer
- Entrepreneur Development of small electronic gadgets based on Microcontroller and VLSI
- Research and Development Professional in Industries and Academics

Title of Unit/Component:

(Detailed Curriculum attached as Annexure-III)

		Means of Assessment			
Outcomes to be assessed	Assessment Criteria for the outcome	Total Marks	Written	Practical	Project
Demonstration of knowledge of Basics of VLSI Design Flow and And Verilog.	Use of basic VLSI Industry related Hardware & software tools. Use of CAD tools in VLSI design. Use and comparison of various VLSI-EDA Hardware-Software tools and their applications.	10	04	06	NO

	Coding in Verilog, Compilation and Execution in System. Design of RTL circuit considering Logic Optimization. Design of a subsystem in a system. Design of functional Analog and digital system in the context of the target hardwere. Design a circuit using EDA tools. Verification and Test Planning of a system				
	Total Marks	10	04	06	NO
Designing of systems based on Programmable Logic Devices (PLDs).	Identify building blocks of a VLSI systems. Integration of various subsystems Debugging, testing systems built around such blocks. Design of subsystems based around PLD Testing of PLD based systems. Comparison w.r.t. Logic Blocks (CLBs), Logic Cells, System Gates, I/O Pins, Flip-Flops, RAM and its type.	10	04	06	NO

	Total Marks	10	04	06	NO
Implementation of FPGA using System Verilog Code Structure.	Data Types, Operators and function used in VLSI.Differentsimulation TechniquesTechniquesusedused in designing.Use of VLSI CAD tools in both digital and analog domainUse ofEDA tools for 	10	04	06	NO
	Total Marks	10	04	06	NO
VLSI Technology: Fabrication & testing of VLSI components.	Identify basic building blocks of VLSI devices. Fabrication & testing of VLSI components. Fabrication of Gyrator Circuit and MOSFET.	10	04	06	
	Total Marks	10	04	06	

VLSI Design us CMOS technology	 sing VLSI circuit design using CMOS technology. Designing and Fabrication of CMOS devices. Calculation of Speed, Area, Power Dissipation and Cost etc 	10	04	06	
	Total Marks	10	04	06	
VLSI Design us SPICE Modeling	sing Use of SPICE tool for simulation.	10	04	06	
	Transient Analysis of				
	CMOS Inverter Level-1,				
	Models.				
	SPICE Modelling for LV				
	Characteristics,				
	Calculation of Capacitance, Parasitic Capacitance, Effective				
	Energy in MOSFET,				
	Designing and simulation of different Analog and				
	Digital systems using				
	different VLSI tool.				
	Total Marks	10	04	06	NO
Creation of Files in var	ious Creation of different files	10	04	06	NO
Format for VLSI Design	n in various Formats while				
	designing of any system their verifications.				
	Total Marks	10	04	06	NO
1		1	1	1	1

Design Verification: Functional and Test Bench Verification using System	Can perform Functional and Test Bench Verification. Coverage Driven Verification, RTL Design Verification of Industry Standard Interface IP and Protocols. Testing of different systems and devices using different VLSI technologies. Testing of various analog and Digital systems and devices.				
	Total Marks	30	10	20	YES
Grand Total	1	100			

Means of Assessment:

- Online assessments carried out using a variety of multiple choice question
- Viva-Voce
- Laboratory works and reports
- Project

Pass/Fail

Following Grading Scheme (on the basis of total marks) will be followed:

Grade	S	Α	В	С	D	Fail
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

SECTION 2

EVIDENCE OF LEVEL

Level of Qualification: 5

OPTION A

	Title/Name of Qualification/Component: Post Diploma in VLSI Desig and Technology						
Outcomes to be assessed	NSQF Domain	Outcomes of the Qualification/Component	How the Job role relates to the NSQF level descriptor	NSQF Level			
INTRODUC TION	Process	After going through this module student will Understand the basics of VLSI, Hardware- Software tools They can Explore the Basics of Verilog. They will gain basic knowledge the of system designing in VLSI	 Students are introduced to the knowledge of the subject, and comprehension is strengthened with interactive Q&A and short quizzes. They will be able to explain and generalize knowledge in VLSI. Students acquire hands-on experience in using CAD tools in VLSI design, and apply what they have learnt in lectures/tutorials to do a mini-project on the design of a subsystem. 	5			
	Professional Knowledge	Student would be able to design different Analog and digital system by synthesis, place, and routing.	 To be able to understand designed functional Analog and digital system To perform synthesis, place, and route of a Mixed signal design into a 	5			

		 target FPGA. To display knowledge of good digital design practices in the context of the target hardware. To learn advanced VLSI design using EDA Tools
Professional Skill	Students would be able to know how to work with EDTA tool for development of VLSI systems using different Hardware and Software	 Handling of EDA 5 tools Hardware and Software for development of VLSI Circuitry. Handling of prototype and pre- production VLSI product for various electronic system and liaise with supplier Able to specify components and equipment required for product development.
Core Skill	Can coordinate with different VLSI companies to design different electronics systems and circuits.	 Providing support 5 for VLSI Design Group Able to give support and advice whenever necessary to all stakeholders

				involved.	
			•	Over the whole product life cycle, Ensure that the products meet the quality standards	
	Responsibility	Responsible for designing different VLSI systems using latest technologies	•	The candidate will learn various aspects of VLSI design	5
Programma ble Logic Devices (PLDs)	Process	They will Understand type of Programmable Logic Devices, FPGA,CLB and flip flops, RAM	•	Students will study the building blocks of a VLSI systems and learn to integrate various subsystems	5
	Professional Knowledge	Will be able to know details of all digital devices and how to do their programming.	•	Students will gain indepth knowledge of Programmable Devices related to VLSI and compatible with various Eco-System.	5
	Professional Skill	Students will be able to find fault in any systems using debugging, testing techniques	•	Student will be able to apply the knowledge in debugging , testing systems built around such blocks	5
	Core Skill	Will have sound knowledge of programmable logic devices for designing the systems	•	Student will be able to handle design of subsystems based around PLD	5

	Responsibility	Responsible for design, verify and testing of any systems	•	Candidate will be able to handle design and testing aspects on PLD based systems.	5
System Verilog Code Structure and FPGA Implementa tion	Process	Will be able to know different functions and Operators used in VLSI Application of pre- processor and its types. Will know simulation Techniques used in designing	•	Students acquire hands-on experience in using CAD tools in VLSI design, and apply what they have learnt in lectures/tutorials to do a mini-project on the design of a sub- system. Student acquires knowledge about working with VLSI CAD tools in both digital and analog domain.	5
	Professional Knowledge	Can difference between designed functional Analog and digital system Will be able to perform synthesis, place, and routing while designing any systems	•	To be able to understand designed functional Analog and digital system To perform synthesis, place, and route of a Mixed signal design into a target FPGA. To display knowledge of good digital design practices in the context of the target hardware.	5

				VLSI design using EDA Tools	
Pi	rofessional kill		•	Handling of EDA tools Hardware and Software for development of VLSI Circuitry.	5
			•	HandlingofprototypeandproductionVLSIproductforvariouselectronicsystemandandliaisewithsupplierforproductionimplementations.	
			•	Support for sales and technical staff.	
			•	Support to areas such as post-design, production & QA.	
			•	Qualitystandardsrequiredfordesigninggoodproduct.	
C	Core Skill	Equipped with Skill related to designing and testing of electronics systems.	•	Providing support for VLSI Design Group	5
			•	Able to give support and advice whenever necessary to all stakeholders involved.	
			•	Over the whole product life cycle,	

		Ensure that the products meet the quality standards	
Responsibility	Will be responsible for translate the customer problem in to real design.	A candidate can translate the problem in to design	5
Process	Will Understand basics of MOS Transistor and different VLSI devices.	 Students are introduced to the knowledge of basic building blocks of VLSI devices, various aspects of design, simulating, fabrication and testing of VLSI components 	5
Professional Knowledge	Gain knowledge related to MOSFET fabrication for Designing of VLSI components	• A student will be able to apply the knowledge for better designing of VLSI components	5
Professional Skill	Will learn the EDTA tool for Designing of different VLSI components	• A student will be able to design VLSI components using various EDA tool.	5
Core Skill	Will develop skill related to tools used for VLSI design	Designing using Different VLSI tool	5
Responsibility	Will be responsible for supporting the VLSI design and testing team when required	• Student will be able to assist the design team in various aspects of VLSI	5

	VLSI Design- Part 1	Process	Will explore the CMOS fabrication technique and its different properties	•	Devices. Students learn the VLSI design style using CMOS Technology. And	5
				various aspects of the subject-speed power dissipation cost etc		
	Professional Knowledge	Gaining basic knowledge of domino logic, Pass Transistor Logic etc. Understanding design style of CMOS with examples	•	Students will be able to correlate and balance the various aspects of CMOS		
		Professional Skill	Will have knowledge related to CMOS designing Can Calculation of Speed, Area, Power Dissipation and Cost	•	Student will gain knowledge related to CMOS designing.	5
		Core Skill	Will be able to design the CMOS and other devices using different techniques.			5
		Responsibility	Responsible for designing of CMOS and other devices.			5
	SPICE Modelling for VLSI Design-Part 2	Process	Understanding SPICE tool for simulation. Knowledge of Power and Energy calculation in MOSFET.			5
			Examples ofSimpleDesignandperforming			

		simulation on them	
		Study of Transfer Characteristics of devices	
	Professional Knowledge	Will have knowledge of Transient characteristics of CMOS Inverter	5
		Will be able to calculate various Capacitance, Resistances in MOSFET	
	Professional Skill	Will develop skill related tom analysis of MOSFET using different characteristics curve and calculations	5
	Core Skill	Will be able to understand the basic design and perform various operations on them. Can design and simulate the electronics systems using SPICE tool	5
	Responsibility	Responsible for designing and simulation of different Analog and Digital systems using different VLSI tools	5
File Interchange Format for VLSI Design	Process	File Interchange Format for VLSI Design Need for File Inter Change, GDS2 Stream, Caltech Intermediate Format (CIF), Library Exchange Format (LEF), Design Exchange Format (DEF), Standard Delay Format (SDF), DSPF and SPEF, Advance Library Format (ALE), Waves Waveform and Vector Exchange Specification, Physical Design Exchange Format, Open Access	5

	Professional Knowledge	 Will gain knowledge related to various File Interchange Format for VLSI Design Will understand types of File Interchange Format used while designing any system. 		5
	Professional Skill	Develop skill related to creation of different files while designing any system.		5
	Core Skill	The main skill they develop will be dealing with different file formats and their verifications.		5
	Responsibility	Responsible for creation of different files while designing of any system		5
Design Verification	Process	They will understand Functional and Test Bench Verification. Understanding Difference between Layout Vs Schematic		5
	Professional Knowledge	Gain knowledge related to different Methodology like OVM, UVM, AVM and ABV used in in VLSI		5
	Professional Skill	Will be able to test different systems and devices using different VLSI technologies.		5
	Core Skill	Will develop skill related to testing and verification of different digital systems.	• Testing of various analog and Digital systems and devices	5

Responsibility	Responsible for Providing support to VLSI Design Group in field of testing and verification.	• Providing support to VLSI Design Group	5

SECTION 3

EVIDENCE OF NEED

What evidence is there that the qualification is needed?

VLSI (Very Large Scale Integration) has emerged as a very significant technology to provide tremendous quantum of process technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvements in performance while achieving reduction in the size, cost and power consumption Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.

What is estimated uptake of this qualification and what is the basis of this estimate?

Based on the experience of NIELIT J&K in this field ,we expect an estimates of around 750 candidates per year in this course

What steps were taken to ensure the qualification (s) does/do not duplicate already existing or planned qualification in the NSQF?

The Qualification does not exist as per information available in public domain.

What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or update?

The Qualification is to be monitored and reviewed every two years. The following data will be used

- Results of assessments
- Employer feedback regarding student skill after conducting a placement drive
- Employer feedback will be sought post-placement
- Student feedbacks
- ✤ Workshops and seminar for reviewing the qualifications
- Consultation/ Tie-up with self help groups, Industries, Expert for review of the Curriculum so as to meet the changing pace of technology and general health care requirements.

Please attach any documents giving further information about any of the topics above.: NIL

SECTION 4

EVIDENCE OF PROGRESSION

After skilling himself through this certification course the incumbent can either start his own enterprise or get associated with any electronic component designing industry. NIELIT shall facilitate forming of small manageable self help groups of such Qualifiers & introduce them at various levels in the various electronic component design, testing services set-up to establish their own manufacturing unit

They shall also be encouraged to take up higher level courses in furtherance of their skill in VLSI and Design.

SECTION 5

EVIDENCE OF INTERNATIONAL COMPARABILITY

List any Comparisons which have been established

- Texas Instruments
- Cypress Semiconductor Corporation
- Analog Device Inc
- Broadcom Corporation
- Cisco Systems
- Bit mapper Integration Technologies Private Ltd
- Horizon Semiconductors
- Trident Tech labs
- HCL Technologies