Simulation and Analysis of Clocked Sense Amplifier using CNFET at 32nm Regime

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INTRODUCTION

The programming technique used in FPGA is SRAM based programming to store the data either 0/1 while selecting the interconnects. The sense amplifier is most important component of semiconductor memory to store the data. As we scale down the transistor size it will be difficult to drive data line so issue it can be overcome by sense amplifier in memory array. When density of memory is redoubled, the bit line capacitance is additionally will increase and due to that, it limits the speed of voltage sense amplifier. Voltage mode sense amplifier during read has been found one of the most promising solutions to reduce the power dissipation and increase the speed. In this paper sense amplifier is analyzed and simulated in a 32nm MOSFET & CNFET technology using HSPICE circuit simulator software.

BASICS OF SRAM MEMORY ARRAY

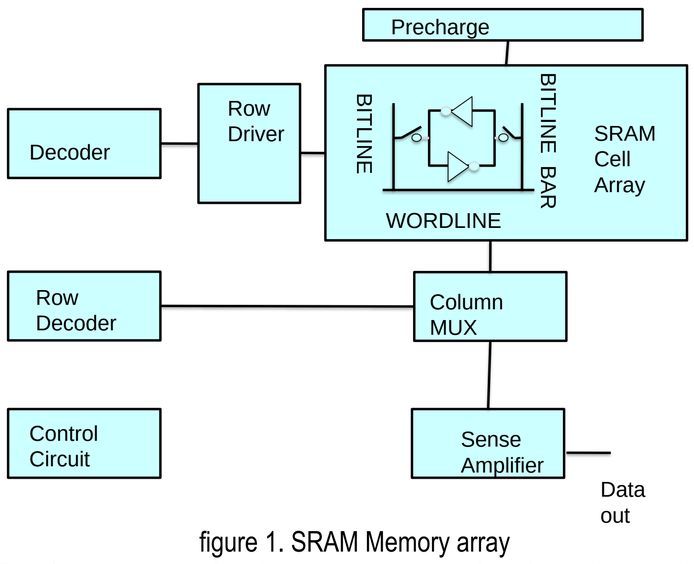


figure 1. SRAM Memory array

To select the one of line from memory array decoder and row driver is connected to SRAM Cell. And other all circuits including sense amplifier is connected to SRAM BLOCK as per figure 1. Pre-charge are used to charge the large line capacitances to the desired level to make operation fast and smooth. Sense amplifiers are used to amplify bit lines differential voltage during read operation without cell data flipping.

IMPORTANT CONCEPTS

1. SRAM Cell

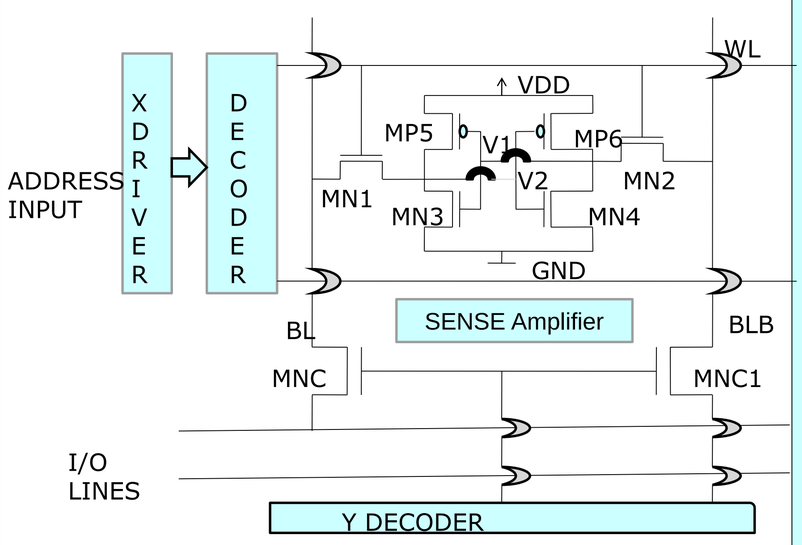


Figure 2 SRAM Cell

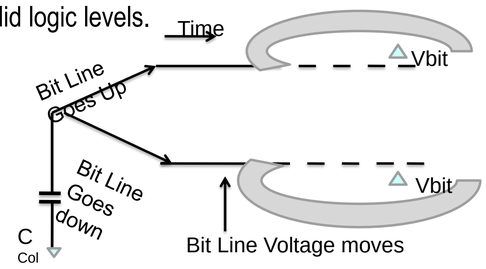
Here we scale down the transistor size upto 32 nm so it will be difficult to drive data line so issue it can be overcome by sense amplifier in memory array.

Read Mode	Write Mode	Hold Mode
1	0	0
0	1	0
1	1	0

IMPORTANT CONCEPTS

2. Sensing Basics

When the row line goes high the data from cell is placed on bit line due to bit line voltage changes. So here bit line looks like capacitor and that only word line goes high at the time in a memory array. Small change in voltage on bit line. So determine the voltage moving upword & down word is chanlage sense amplifier to drive the bit line to full valid logic levels.

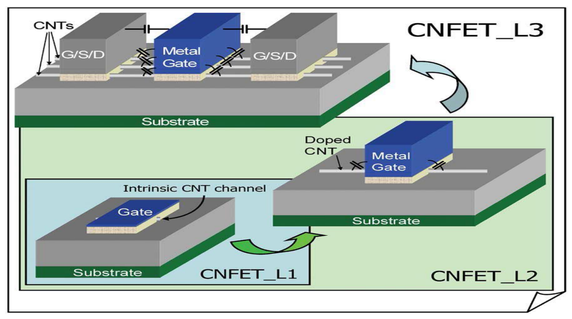


CNFET

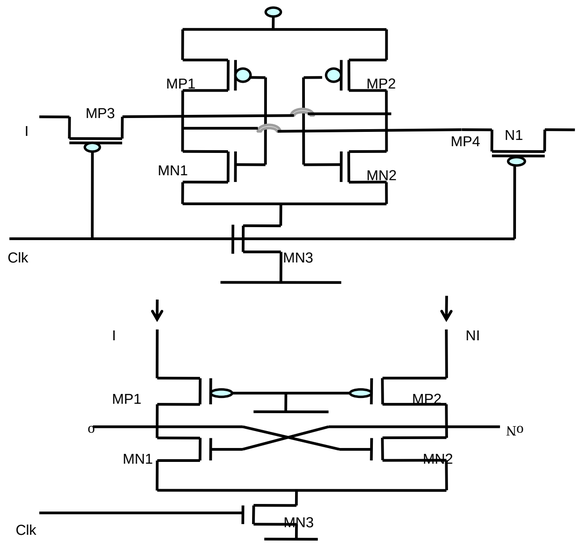
Here in CNFET having promising device that avoids most of the limitations of the traditional silicon MOSFET. The quasi-1-D structure provides better electrostatic control over the channel region than 3-D device (e.g., bulk CMOS) and 2-D device (e.g., fully depleted SOI) structures. In level one CNFET denotes CNFET_L1 similar to intrinsic device like MOSFET.

In the second level CNFET_L2, includes the device non idealities: the capacitance and resistance of the doped S/D CNT region, as well because the doable SB resistances of S/D contacts. The first two levels cope with just one CNT beneath the gate.

The top level, denoted as CNFET_L3, models. This level deals Figure 1 Cross-sectional area along CNTFET used in simulations with multiple CNTs per device and includes the parasitic gate capacitance and screening due to the adjacent CNTs.



SENSE AMPLIFIER DESIGN



The Transistors MP1, MP2, MN1, and MN2 form a cross-coupled complementary structure.

Clock Is low (MN3)	MP3 & MP4 on	Output is not valid
Clock is High	Transistor state depends on input	Voltage change approximately 10%

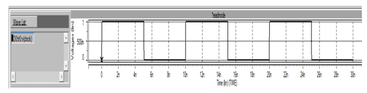
Here input signal is always maintained to VTHP without off the MP3 and MP4. Assume that input signal is above VTHP the drain of MN1/MP1 and MN2/MP2 are changes to I and NI. When clock is low, the circuit outputs are not valid logic signals but rather, ideally, track the input signals.

RESULTS

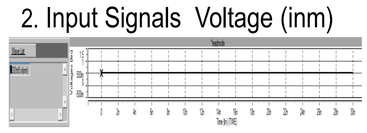
MOSFET RESULTS

Using 32nm CMOS & CNFET technology we have simulate the Clocked Sense amplifier output and obtain the following waveform.

1. Clock

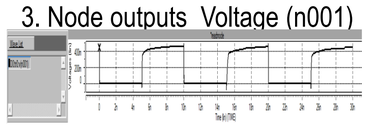


2. Input Signals Voltage (inm)

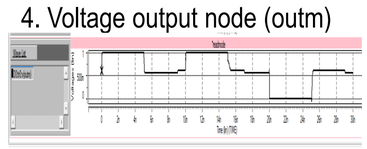


Voltage (inp)

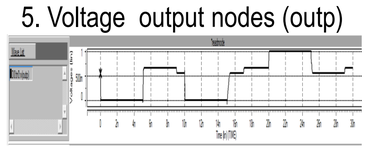
3. Node outputs Voltage (n001)



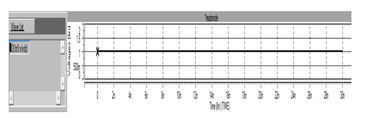
4. Voltage output node (outm)



5. Voltage output nodes (outp)

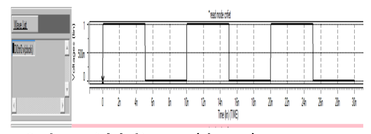


6. Vdd

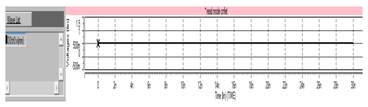


CNFET output voltages

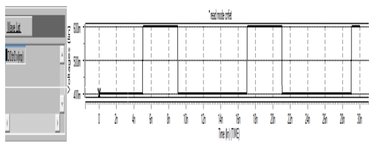
1. Clock



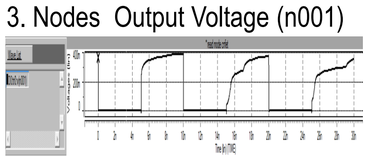
2. Input Voltage (inm)



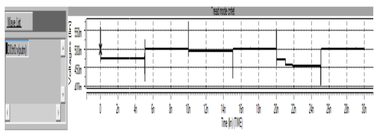
Voltage (inp)



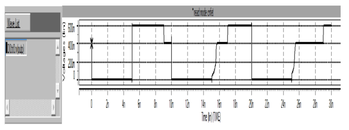
3. Nodes Output Voltage (n001)



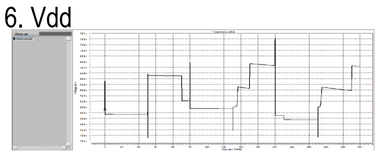
4. Voltage Output node (outm)



5 Voltage output nodes (outp)



6. Vdd



MOSFET SENSE AMPLIFIER	CNFET SENSE AMPLIFIER SIMULATION
Voltage (inm) = 0.5 v	Voltage (inm) = 5.000e-01 v =1.83v
Voltage (inp) = 0.4 v	Voltage (inp) = 4.000e-01 v =1.47v
Voltage (n001) = 0.44 v	Voltage (n001) = 3.652e-01 v =1.34v
Voltage (outm) = 0.61 v	Volatge (outm) = 5.000e-01 v =1.83v
Voltage (outp) = 0.55 v	Voltage (outp) = 4.000e-01 v =1.47 v
Voltage (Vdd) = 1.0000 v	Voltage (Vdd) = 4.908e-01 v =1.80v

CONCLUSION

As we observe due to the high clock pulse improvement in the voltage also it increases the speed. The CNFET Clocked Sense amplifier improves the results up to 10% than the conventional CMOS Sense Amplifier. Here we have simulated the CNFET Sense amplifier by comparing the readings of the MOSFET we observe that the CNFET Sense amplifier having less delay.

FUTURE SCOPE

This circuit is plagued with problems including: kickback noise.

REFERENCES

❖www.researchgate.net/publication/296467448_Optimization_and_Analysis_of_6T_SRAM_using_CNFET_at_32nm_Regime

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