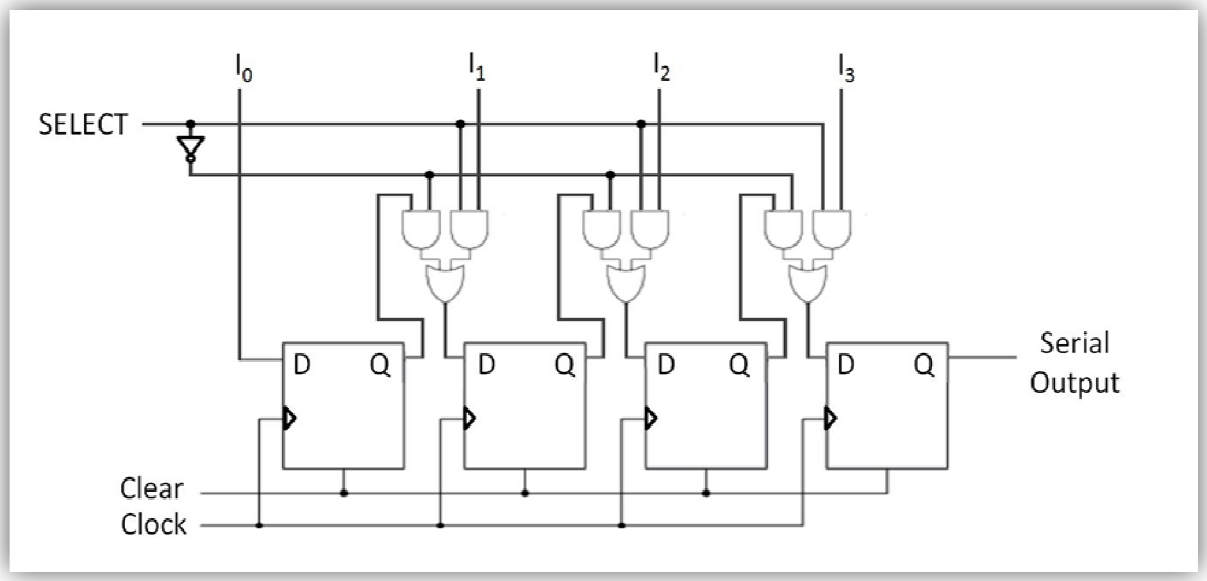
Course Name: A Level (1st Sem) **Subject: CO**

Topic: Registers contd. **Date: 31-03-20**

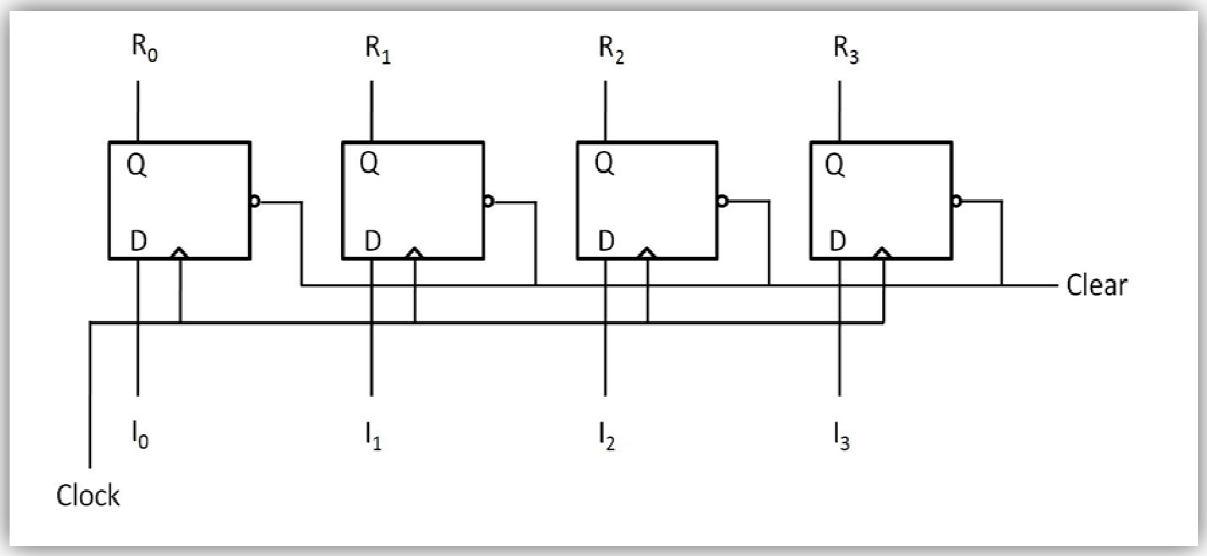
Parallel In – Serial Out Shift Registers: A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops, AND Gates & OR gates for entering data (i.e. writing) to the register. I_0, I_1, I_2 and I_3 are four parallel inputs. Except for the Flip-Flop storing LSB bit, every other Flip-Flop needs a MUX that can SELECT either fresh input or the shifted bit from Least Significant Position.



Here as we see in this diagram, first flip-flop gets a fresh input (I_0), but the second is given two options- either to get fresh input (I_2) or to get output (Q) of previous flip-flop. This is literally what we call parallel input but serial output.

Parallel In – Parallel Out Shift Registers: A Parallel Input – Parallel Output Shift Register is very similar to a simple register that takes discrete inputs and provides discrete outputs. Here I_0, I_1, I_2 and I_3 are the inputs and R_0, R_1, R_2 and R_3 are the outputs. A Clock input is used to initialize the circuit and a Clear input is used to clear the Flip-Flops at any moment.

Here as we see in the diagram, every flip-flop gets fresh input, and every flip-flop provides discrete output. Since all inputs and outputs are discrete, we call it parallel input and parallel output register.



Assignments:

1. Construct a 6-bit PISO register. Why do we need MUXes in these registers?
2. How is SIPO different from PIPO? Explain in brief.