Course Name: A Level (1st Sem) **Subject: CO**

Topic: Complete Computer Description **Date: 22-05-20**

The complete computer description includes both, the instruction cycle and the interrupt cycle. Interrupt cycle because there may arise a case of I/O operation anytime during normal operation. Instruction cycle because in absence of interrupts, the CPU is always busy with stored program instructions. A flip flop R is used as a condition to determine the type of operation. When R=0, the instruction cycle continues. Similarly when R=1, the computer goes through an interrupt cycle. *Here it must be noted that an interrupt signalled by IEN and R is just to make it sure that another interrupt does not get entertained while processing of an interrupt.*

A basic computer consists of the following hardware components:

- A memory unit of 4096 X 16 bits
- Nine Registers- PC, AR, IR, DR, AC, TR, INPR, OUTR and SC
- Five Flip-Flops- I, R, IEN, FGI and FGO
- Two decoders- a 3 to 8 operation decoder and a 4 to 16 timing decoder
- A 16-bit common bus
- Control Logic Gates
- Arithmetic and Logic Unit connected to AC

Control functions and micro operations for a basic computer are as follows:

Instruction Cycle

Fetch Phase:

$R'T_0$: $AR \leftarrow PC$

$R'T_1$: $IR \leftarrow M[AR], PC \leftarrow PC + 1$

Decode Phase:

$R'T_2$: $D_0 \ldots .D_7 \leftarrow$ Decode IR[12-14],
$AR \leftarrow IR[0\text{-}11]$,
$I \leftarrow IR[15]$

Indirect address in Memory Reference Instructions:

$R'T_0$: $AR \leftarrow PC$

$R'T_1$: $IR \leftarrow M[AR], PC \leftarrow PC + 1$

Interrupt Cycle

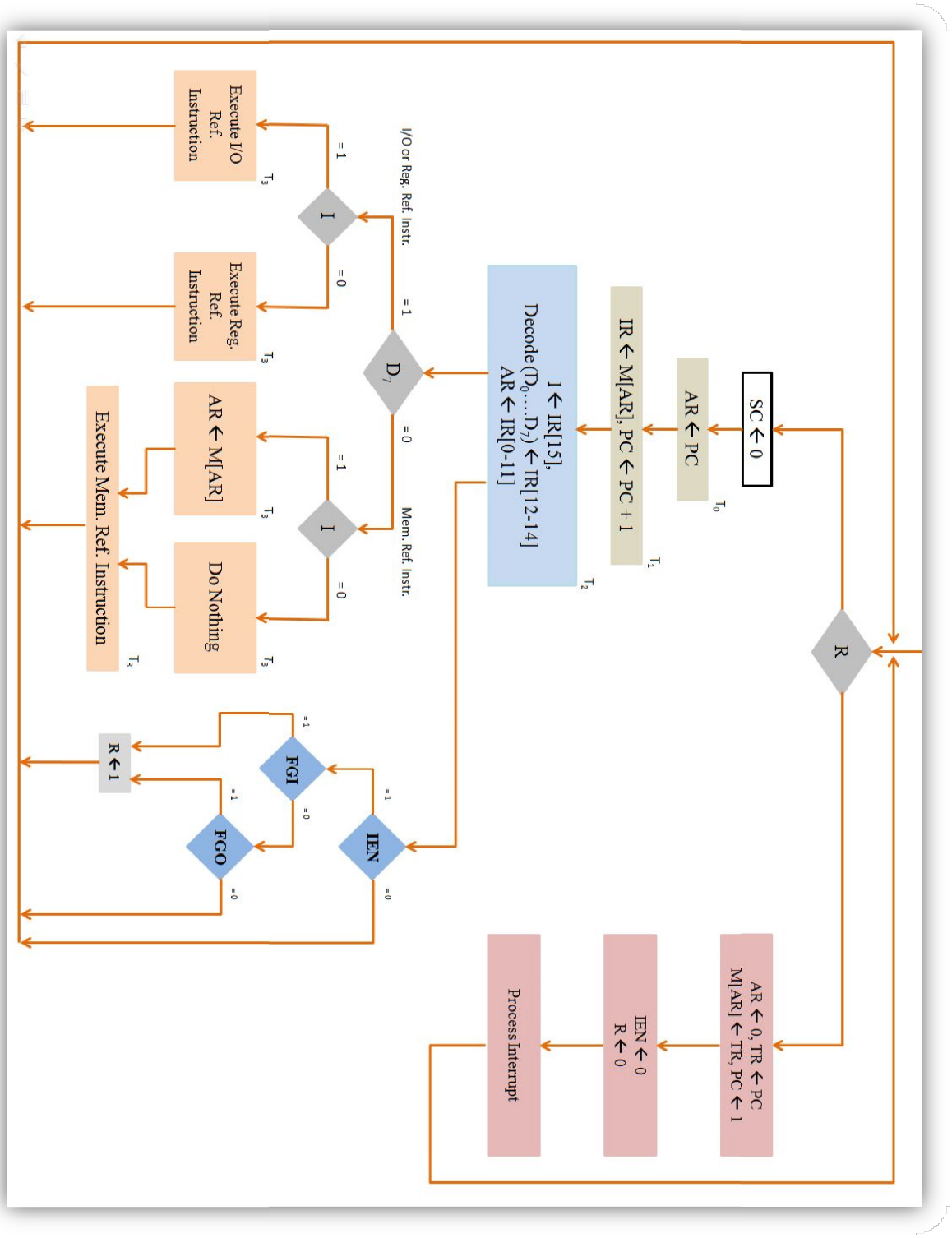
$T_0' T_1' T_2' (IEN) (FGI + FGO) :$ $R \leftarrow 1$

$R T_0 :$ $AR \leftarrow 0, TR \leftarrow PC$

$R T_1 :$ $M[AR] \leftarrow TR, PC \leftarrow 1$

$R T_2 :$ $IEN \leftarrow 0, R \leftarrow 0$

Consider the following diagram: (Rotated at 90° for convenience in reading)



Assignment:

1. List out the necessary components that are needed to form a basic computer.
2. Discuss about all the necessary RTL statements related to simple Instruction Cycle.