Course Name: A Level (1st Sem) **Subject: CO**

Topic: Instruction Cycle **Date: 20-05-20**

Instruction Cycle: Instruction Cycle is a detailed procedure using which; an instruction triggers and completes its execution. Usually a computer works with 16-bit instruction code which is further divided into 3 significant parts- the Mode Bit, the Opcode and the Address of operand. Each of these parts must be decoded by the control unit so that the execution can take place.

The entire procedure is divided into following three phases-

1. Fetch Phase
2. Decode Phase
3. Execute Phase

Fetch Phase: Fetch phase refers to the extraction of a new instruction from memory to the Instruction Register (IR). For this to occur, the memory address of the instruction is transferred into Program Counter (PC) by the control unit. PC then transfers the address to Address Register (AR). AR now explores the memory and extracts the instruction.

The extracted instruction is transferred to IR and PC gets an increment of 1. Increment of PC refers to the subsequent pointing towards the next instruction in memory. Consider the following RTL notations-

$$AR \leftarrow PC$$
$$IR \leftarrow M[AR], PC \leftarrow PC + 1$$

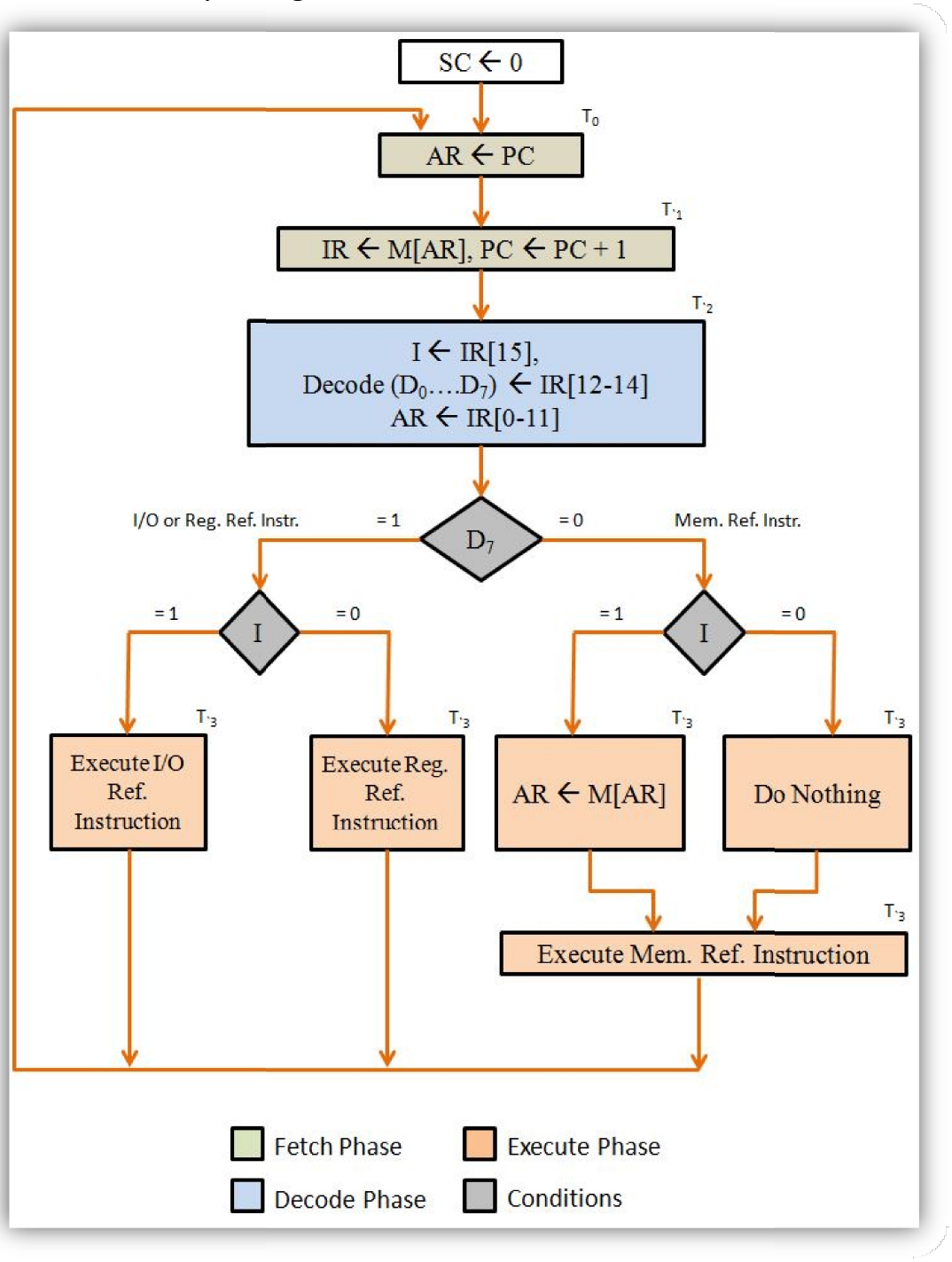
Decode Phase: Decode phase starts after instruction is stored in IR. The first thing to decode is Mode Bit. It is transferred in a separate flip-flop I. Next is to decode the 3-bit Opcode which is done using a 3 to 8 decoder. D_7 output of the decoder is- when 1, denotes that the Opcode was 111.

Thus the decoder output along with I flip-flop determine whether the instruction was a Memory Ref. Instruction or not. In concurrence, the 12 bit Operand address is transferred into AR so that the operand can be fetched out of memory. Consider the RTL notations-

$$I \leftarrow IR[15],$$
$$Decode\ (D0....D7) \leftarrow IR[12\text{-}14]$$
$$AR \leftarrow IR[0\text{-}11]$$

Execute Phase: Execute phase starts after the instruction is decoded completely. The operand is fetched out from memory during this phase and rest of the process is accomplished by arithmetic and logic circuits. Fetching of operands depend upon the mode of address being used in the instruction.

The complete instruction cycle is given below-



Assignment:

1. In brief, explain the different phases of Instruction Cycle.