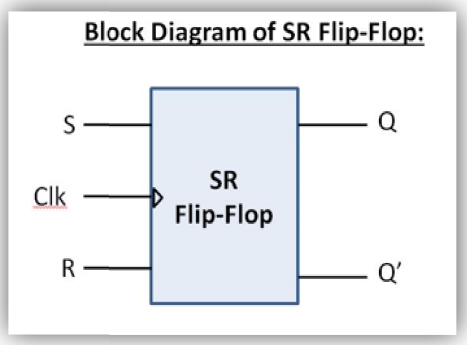
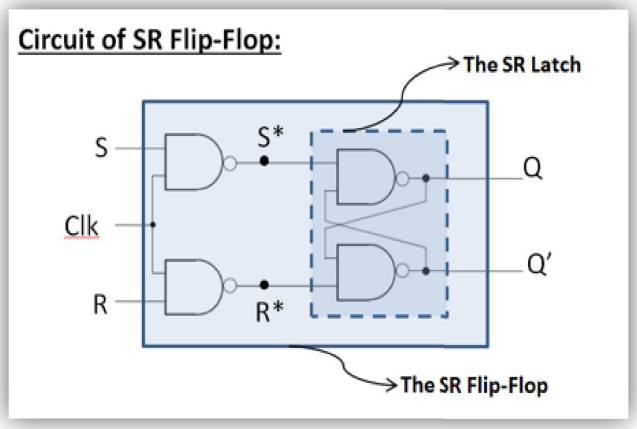
Course Name: A Level
Topic: Flip-Flop Contd.

Subject: CO
Date: 20-03-20

SR (Set-Reset) Flip-Flop:

As its name implies the SR Flip-Flop works for just two states. Either it SETs (stores 1 to the Latch) or it RESETs (stores 0 to the Latch). Although a Flip-Flop can be constructed by any of the two types of Latches, but the best practice is to use NAND gate Latch. The circuit and Truth Table of SR Flip Flop are given here:



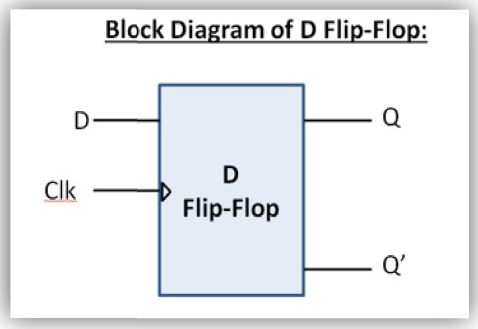


Truth Table:

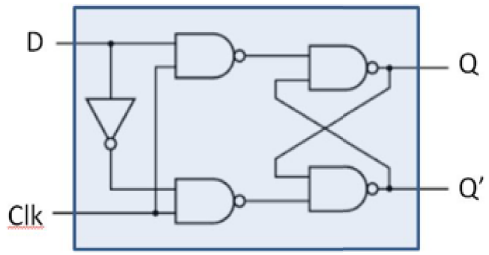
Clk	S	R	S*	R*	Q	Q'
0	X	X	X	X	X	X
1	0	0	1	1	0	1
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	1	0	0	1	1

D (Delay) Flip-Flop:

D Flip-Flop is a slight modification of SR Flip-Flop. Since SR flip flop suffers from an unavoidable condition called NO VALUE or RACE CONDITION. D Flip-Flop is designed to avoid it. The D input to this Flip-Flop is sole input and is inverted to create a set of two necessary inputs. This management disables the similar input combinations like [0,0] or [1,1] and only SET, RESET outputs are evaluated.



Circuit of D Flip-Flop:

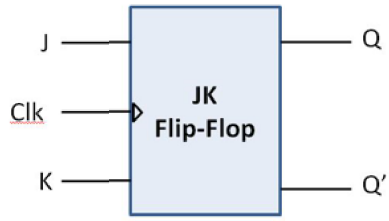


Truth Table:

Clk	D	S*	R*	Q	Q'
0	X	X	X	X	X
1	0	1	0	0	1
1	1	0	1	1	0

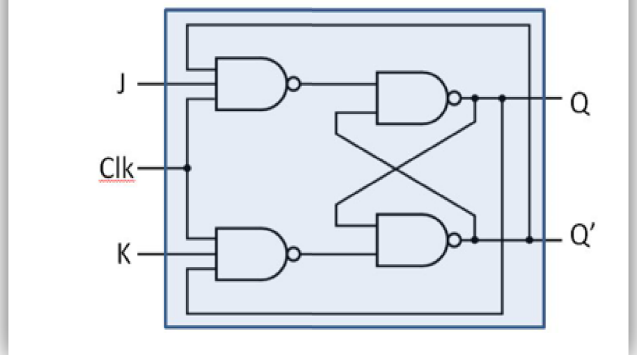
JK (Jack Kilby) Flip-Flop:

Block Diagram of JK Flip-Flop:



The JK flip-flop is basically an SR flip-flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time thereby eliminating the RACE CONDITION seen previously in the SR flip flop circuit. Also when both the J and the K inputs are at logic level "1" at the same time, and the clock input is pulsed either "HIGH", the circuit will "toggle" from its SET state to a RESET state, or visa-versa.

Circuit of JK Flip-Flop:



Truth Table:

Clk	J	K	Q
0	X	X	X
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	Q'

Assignments:

1. Describe the functioning of SR Flip-Flop with Truth Table.
2. How is JK different from SR Flip-Flop?