<u>Course Name: A Level (1st Sem)</u> <u>Topic: Counter</u>

<u>Subject: CO</u> <u>Date: 01-04-20</u>

Binary Counters: The external clock pulses (pulses to be counted) are fed directly to each of the J-K flip-flops in the counter chain and both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, logic is set to "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.



<u>Clock Diagram for 4-bit Binary Counter:</u> Following is a diagram that clearly shows the TOGGLING effect of JK Flip-Flop on this counter. We can see that the Right most Flip-Flop works as for LSB bit while the Left most bit works as for the MSB bit. Thus Q3 toggles every-time when FF3 sets to 1. Q2 toggles every-time when FF2 sets to 1 and so on.



Assignments:

- **<u>1.</u>** Construct a 5-bit counter. Also write the entire counting sequence generated by it.
- 2. Why JK is used for counters?