Course Name: A Level (1st Sem) Subject: CO

Topic: Modes of Transfer contd. Date: 11-06-20

DMA Transfer → In a hardware with DMA mechanism, peripherals put their data on to their interfaces and get acknowledged. DMA controller now makes a request for granting access of the FSB (Common Bus) by using a line BR., BR takes the request to CPU when CPU grants the access, it makes a line BG as 1.

When BG is 1 DMA controller comes to know that the common bus can be used for transfers. Since it is a parallel processor, it uses all the line needed to read from or write in to the memory it places the address on address line data on input line and when write enable is made 1 the data is transfer to memory. CPU is bypassed here by.

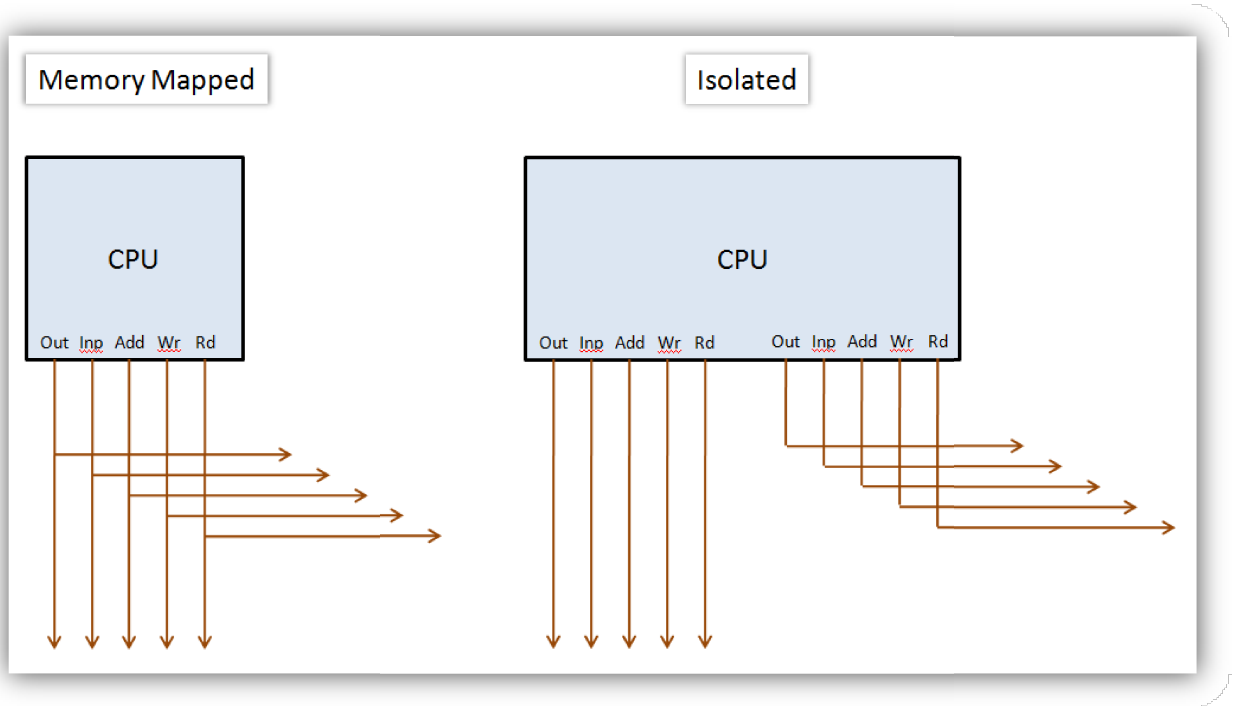
Cycle stealing → By default every transfer is a process and it should be accomplished by a CPU. Programmed I/O and interrupt initiated I/O are the two transfer method in which transfers are performed the same processor that is working for general operations but in DMA we have a seperate processor DMA controller for handling transfers. Considering every succesful transfers that are handled by DMA are called stolen cycles since CPU is not much involved in these transfers this mechanism is called cycle stealing.

Isolated V/s Memory mapped → Usually CPU use the same line for r/w as memory chips use. But when some kind of I/O transfer is involved, the scenario gets changed. there may be any of the following two method.

Memory mapped I/O → In this method every line (input, output, address, read, write) are common for memory transfer & I/O transfer although it makes a burden on the involved line of the common bus. CPU uses time divisions to perform both operation simultaniously.

Isolated I/O → In this method the burden of common bus is reduced by increasing lines.

A CPU in this mechanism uses seperate lines of trasfer for memory & I/O. input, output, read & write lines are seperate for memory & I/O and this arrangement isolates all I/O transfers from memory transfers. Minwhile address lines are common to both



Interrupt Priority→ While processing interrupt a flip-flop 'R' is used to avoid some other interrupt inside the one that is being processed but if two interrupt different devices come at the same time, we need a priority to determine which will be process first. Following are two method for managing it-

1- Default priority of hardwares
2- Daisy chaining

Mostly hardware manufacturers define a particular priority for the hardware and this priority works when interrupts from those hardware occurs like wise peripherals likes keyboard mouse etc. have lower priority than disk drives like FDD, HDD, etc. Stil in peripherals devices enjoy higher priority than printing devices.

Dasichaining is another method that drametically handles the situation when two or more interrupt of same priority occure at the same time in this method interrupting devices are scheduled to operate in an enclosed chain method. Every devica is given equal slot to process its interrupt.

NOTE: This content is entirely written, diagrammed and prepared by me [Shashi Kant Mani Tripathi], hence you can write it all in your notes as it is.

Assignment:

1. Differentiate between Memory Mapped I/O and Isolated I/O.
2. Briefly describe Interrupt Priority.